OSNOVE DIGITALNE ELEKTRONIKE

Bistabili

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Bistabili

Ishod učenja 7 - Uvod u sekvencijske sklopove

Sadržaj predavanja

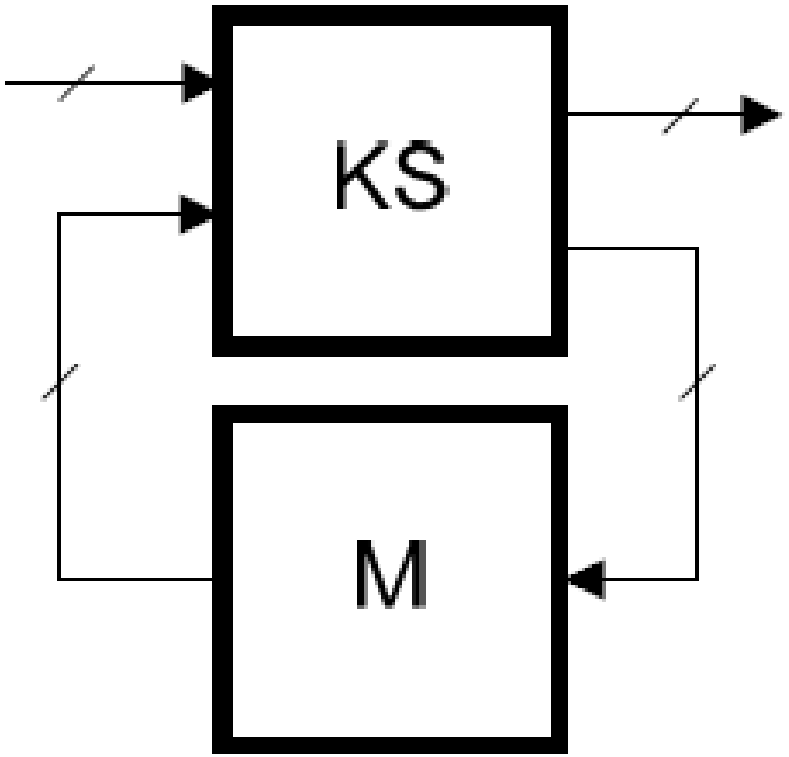
- Sekvencijski sklopovi
- Asinkroni i sinkroni bistabili
- Tipovi bistabila (RS, JK, T, D)
- Upravljanje bistabilima (CP)
- Upravljanje sekvencijskim sklopovima razinom i bridom

Uvod

- Kombinacijski sklopovi nemaju svojstvo pamćenja
- Izlaz postoji samo kad postoji i ulaz
- Da bi logički sklop mogao pamtiti ulaznu vrijednost varijable mora imati **logičku povratnu vezu**

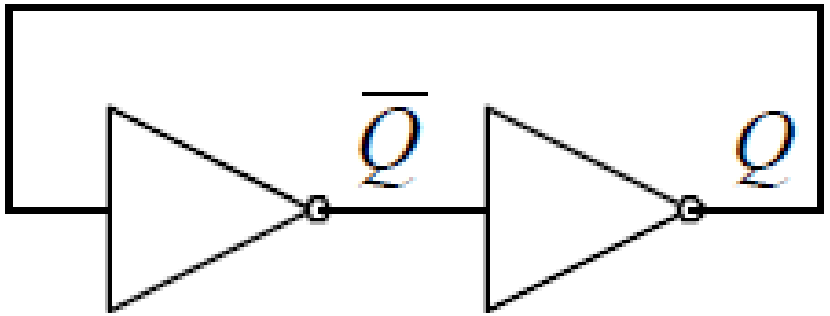
Struktura sekvencijskog sklopa

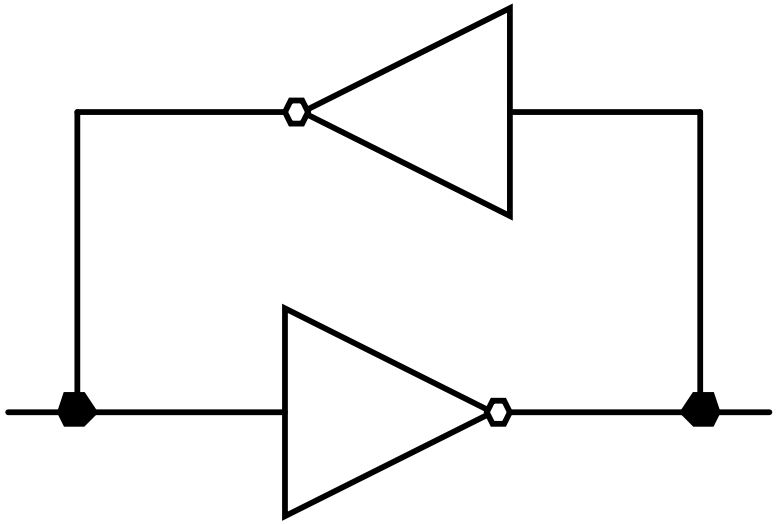
- Kombinacijski dio (KS)
- Memorija (M)
  - dva stabilna stanja omogućuju pamćenje binarne vrijednosti



Bistabil

- Sklop s dva stabilna stanja
- Stanje se može promijeniti samo pomoću vanjskog impulsa
- Može pohraniti (zapamtiti) jedan bit informacije
- U širokoj je upotrebi u digitalnoj logici i računalnoj memoriji

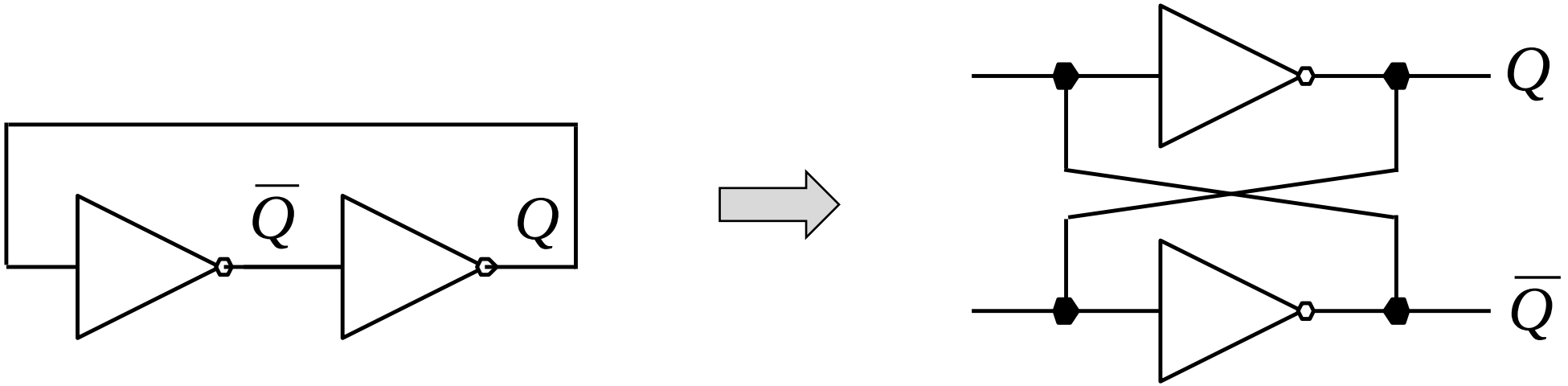




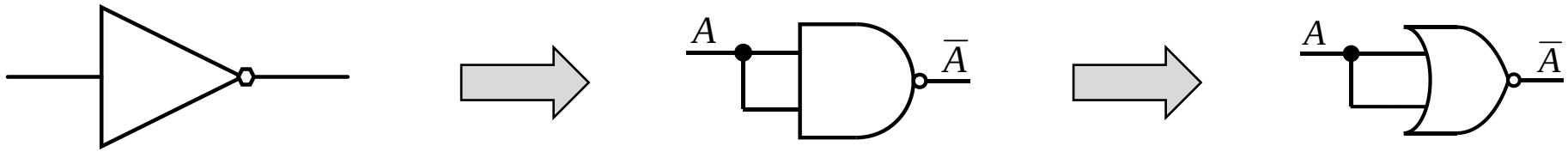
Osnovni spoj bistabila

Bistabil ostvaren logičkim sklopovima:

- električka i "logička" povratna veza
- Logička struktura za pohranu informacija

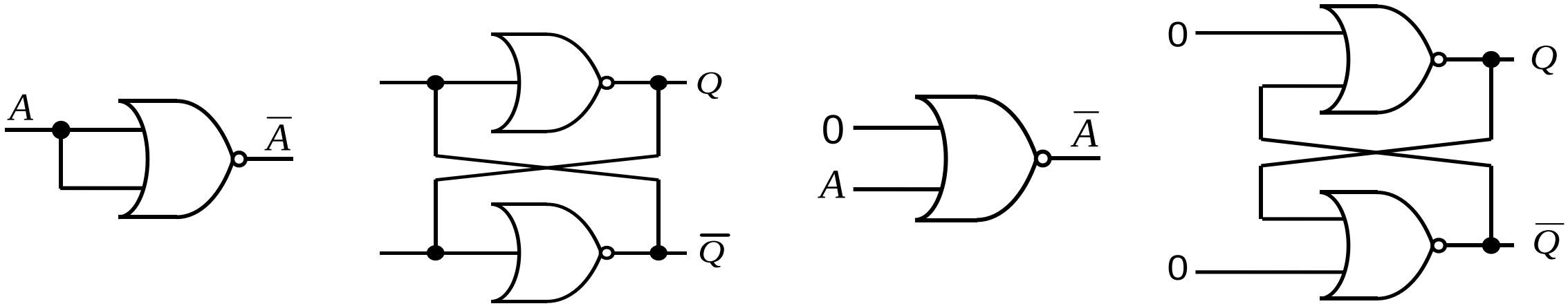


Invertor s NI i NILI funkcijama

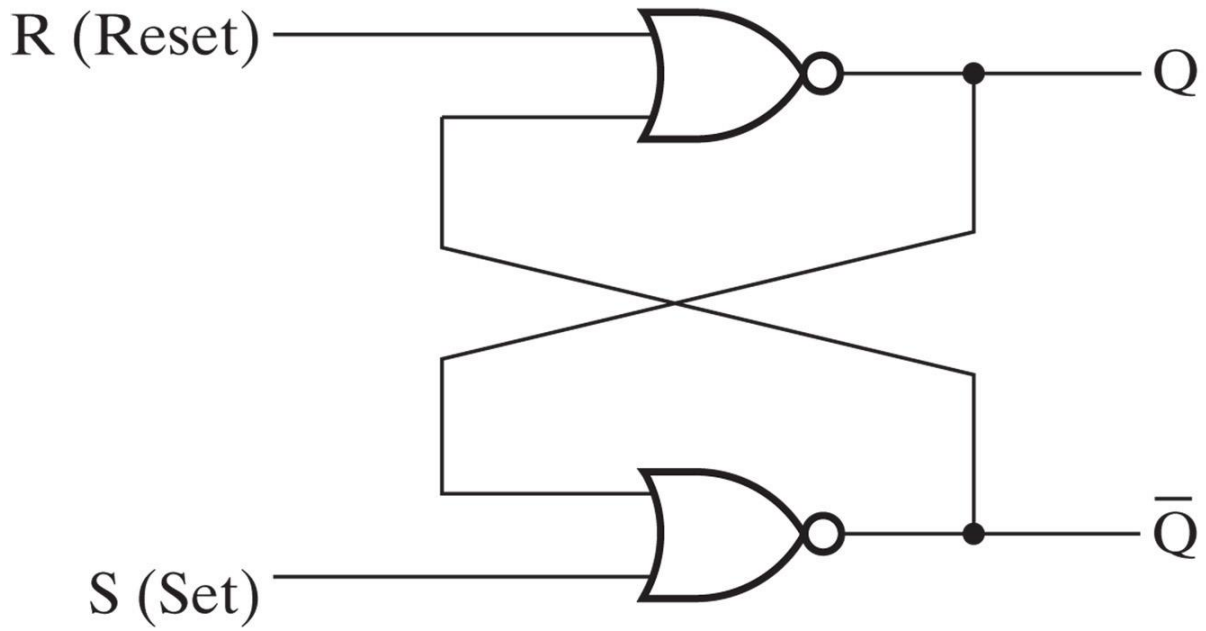


- Univerzalne funkcije omogućuju upravljanje bistabilom

Bistabil ostvaren NILI logičkim sklopovima



Bistabil ostvaren NILI logičkim sklopovima

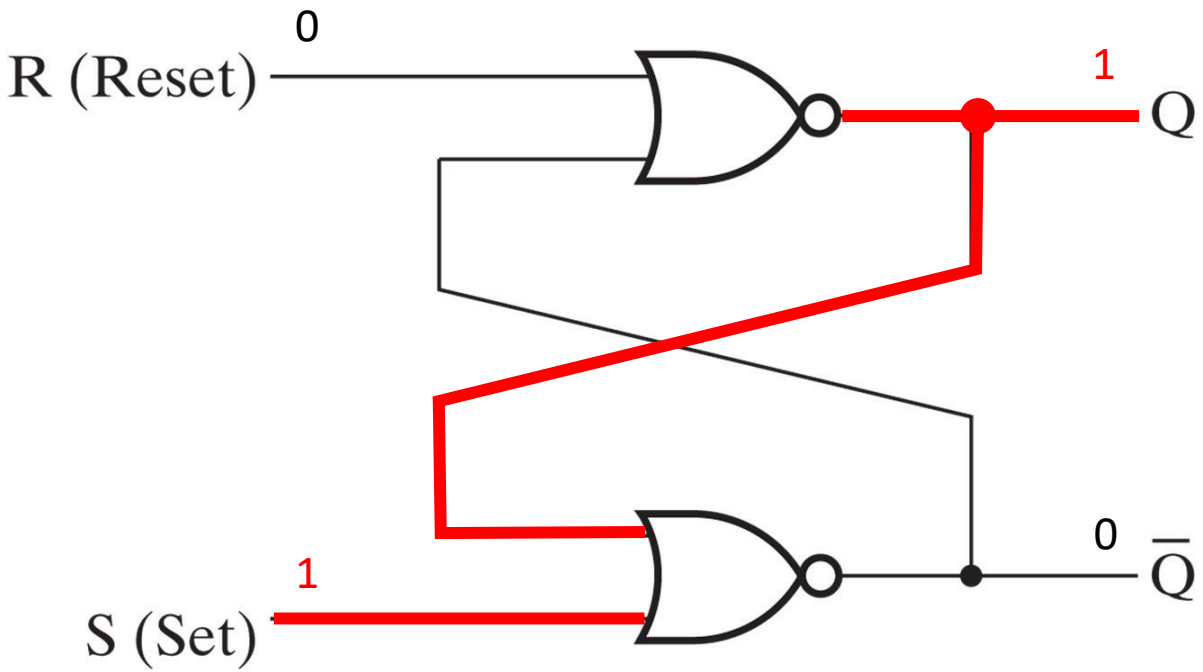


(a) Logic diagram

S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

(b) Function table

Bistabil ostvaren NILI logičkim sklopovima

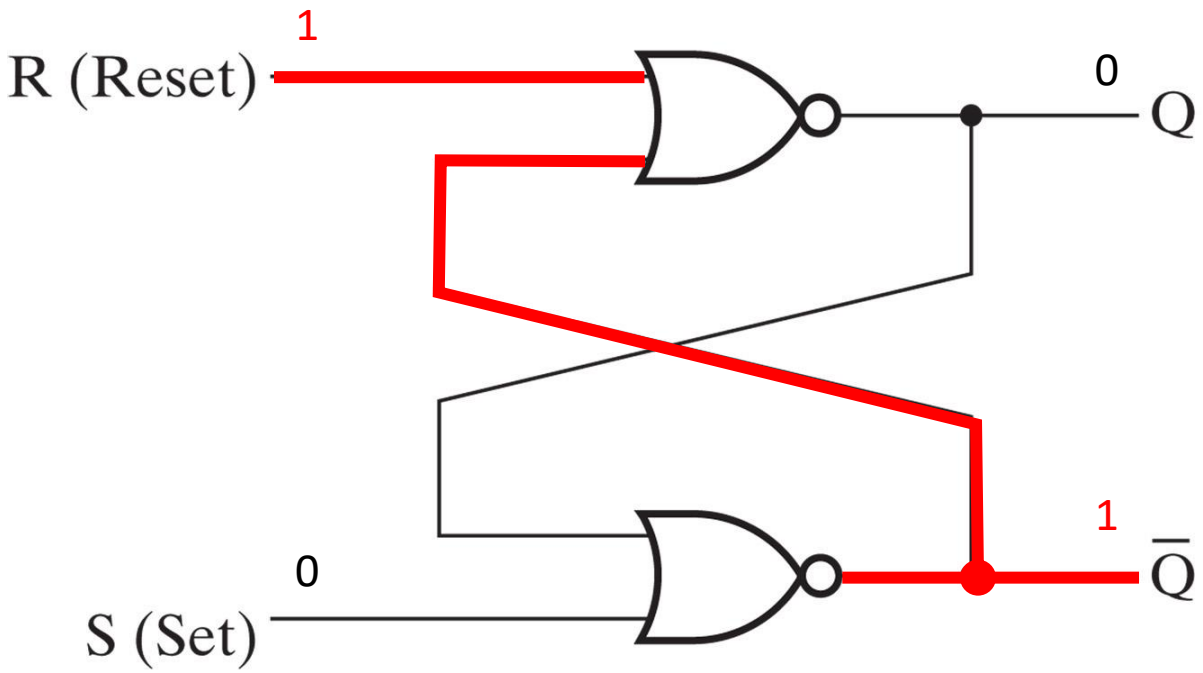


(a) Logic diagram

S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

(b) Function table

Bistabil ostvaren NILI logičkim sklopovima



(a) Logic diagram

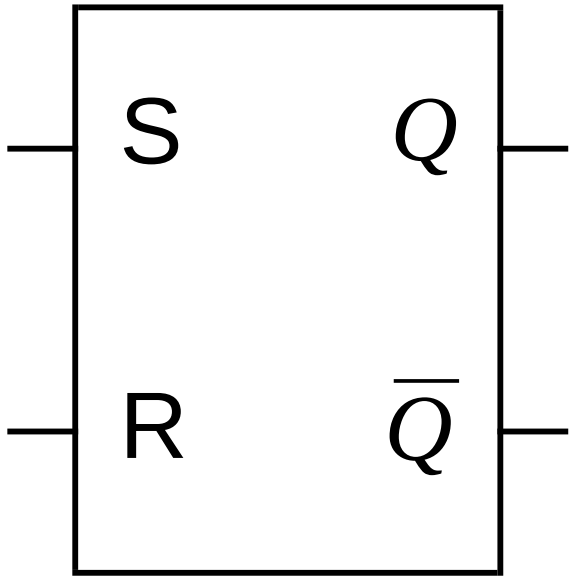
S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

(b) Function table

Simbol bistabila

Izlazi:

- Q izlaz
- $\overline{Q}$ komplementarni izlaz

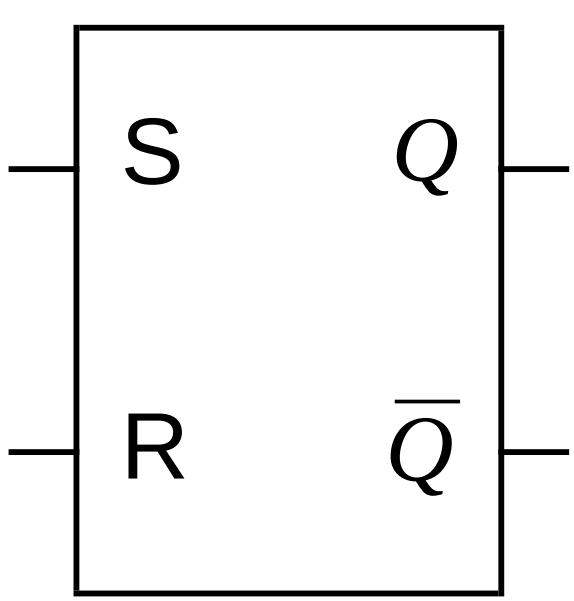


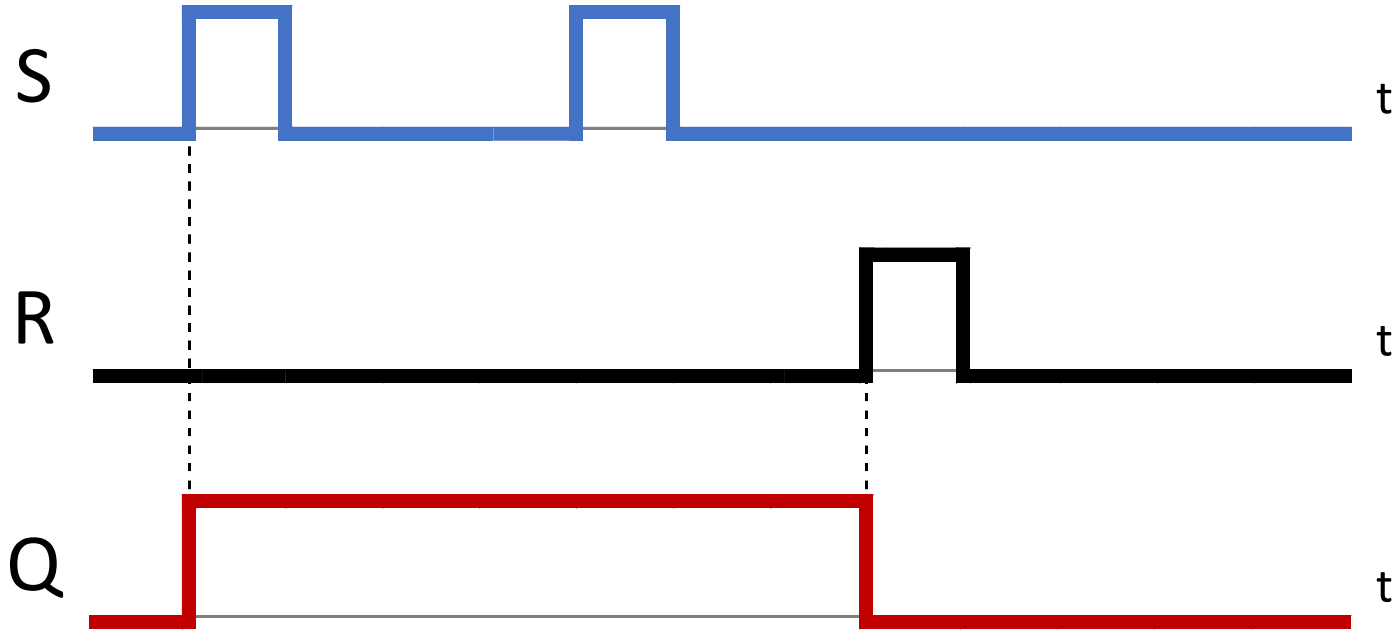
Ulazi:

- **S** [set] postavljanje Q = 1
- **R** [reset] "brisanje"! Q = 0

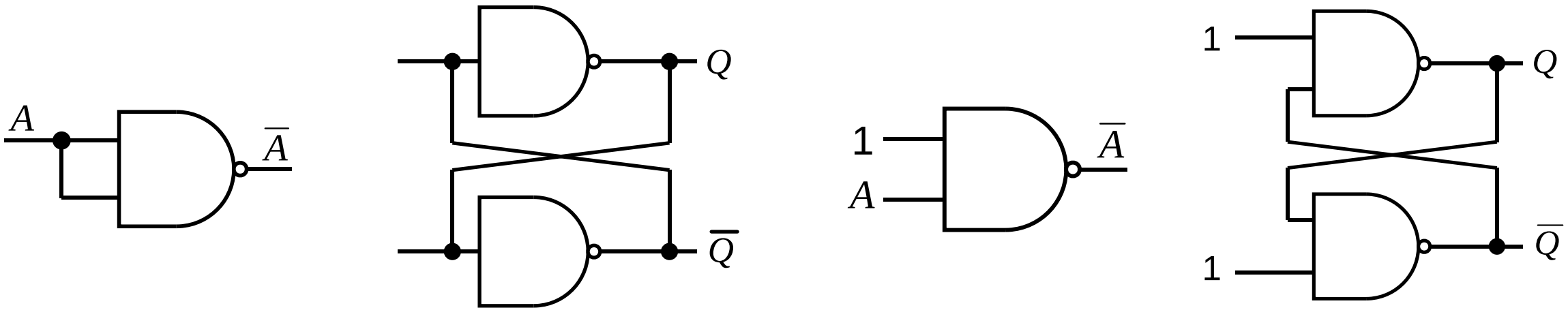
Ponašanje bistabila

- Djelovanje impulsa na jednostavni SR bistabil

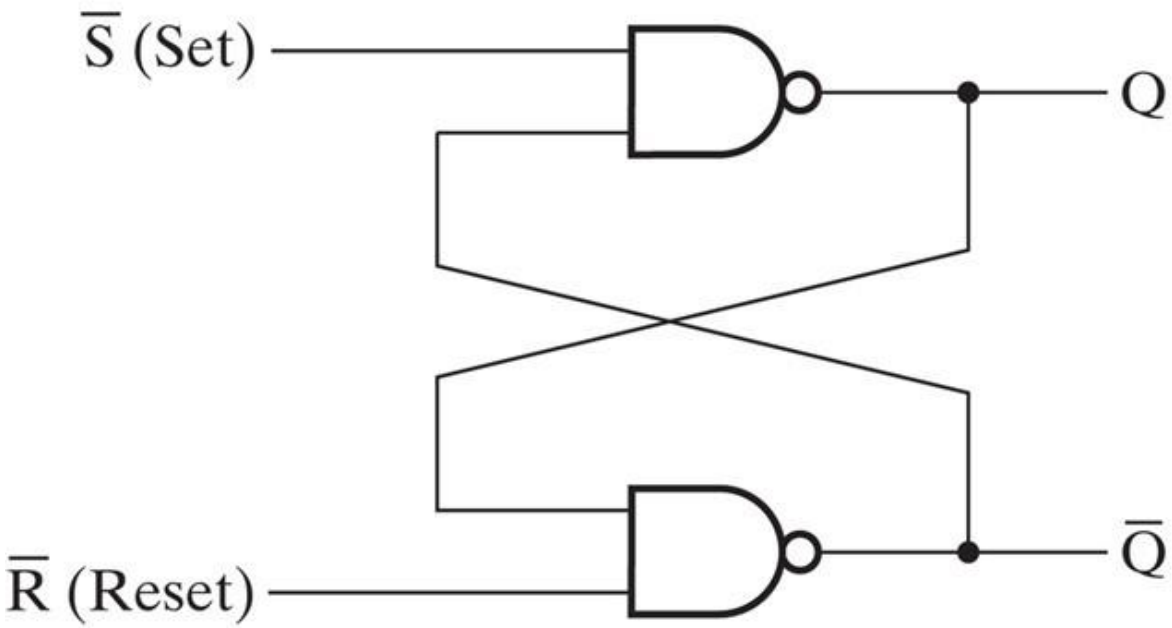




Bistabil ostvaren NI logičkim sklopovima



$\overline{S}\,\overline{R}$ bistabil ostvaren NI logičkim sklopovima

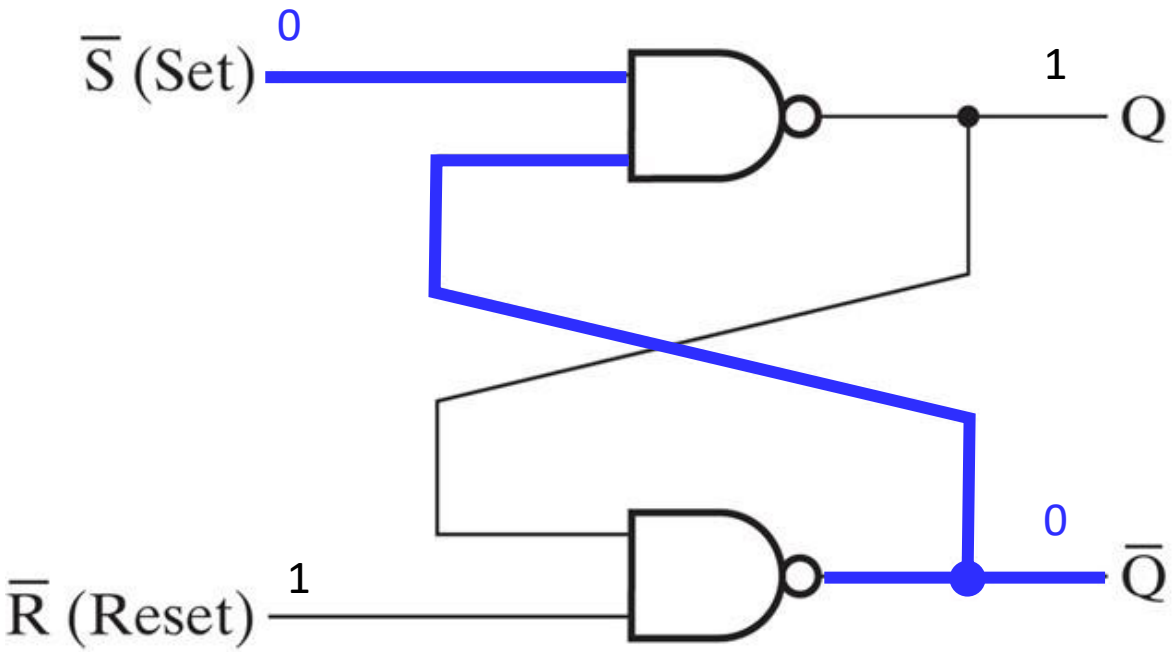


(a) Logic diagram

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	1	1	0	Set state
1	1	1	0	
1	0	0	1	Reset state
1	1	0	1	
0	0	1	1	Undefined

(b) Function table

$\overline{S}\,\overline{R}$ bistabil ostvaren NI logičkim sklopovima



(a) Logic diagram

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0	1	1	0	Set state
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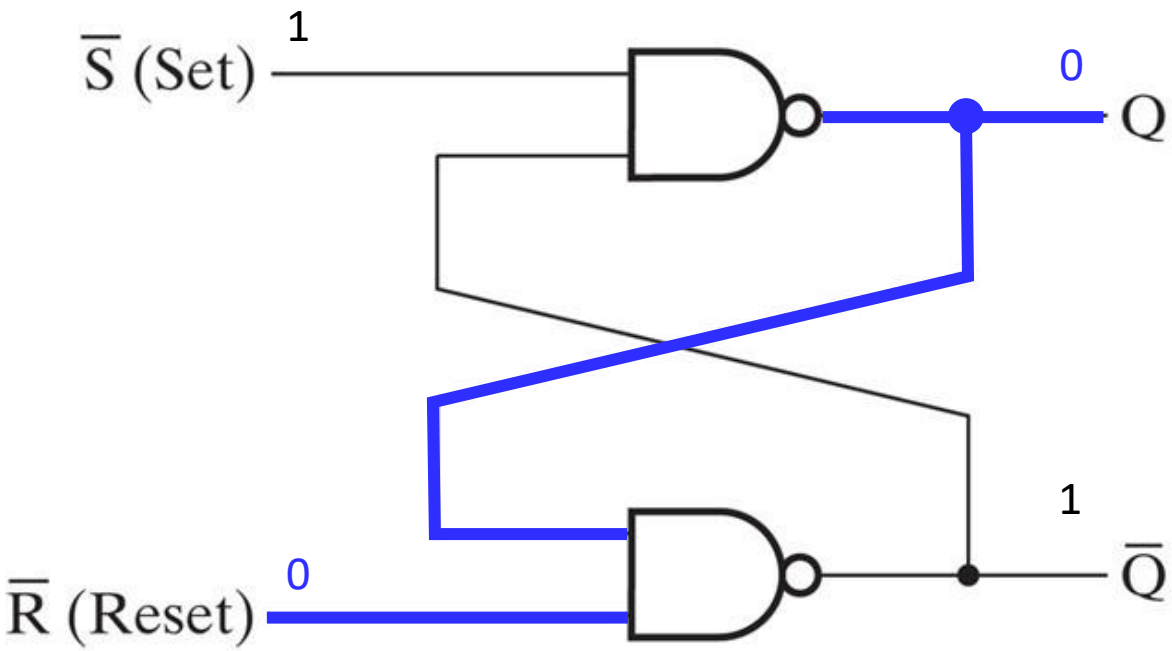
(b) Function table

$\overline{S}\,\overline{R}$ bistabil ostvaren NI logičkim sklopovima

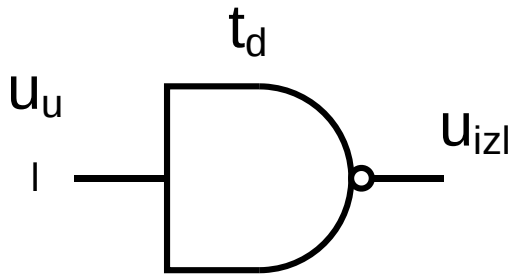


(a) Logic diagram

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	1	1	0	Set state
1	1	1	0	
1	0	0	1	Reset state
1	1	0	1	
0	0	1	1	Undefined

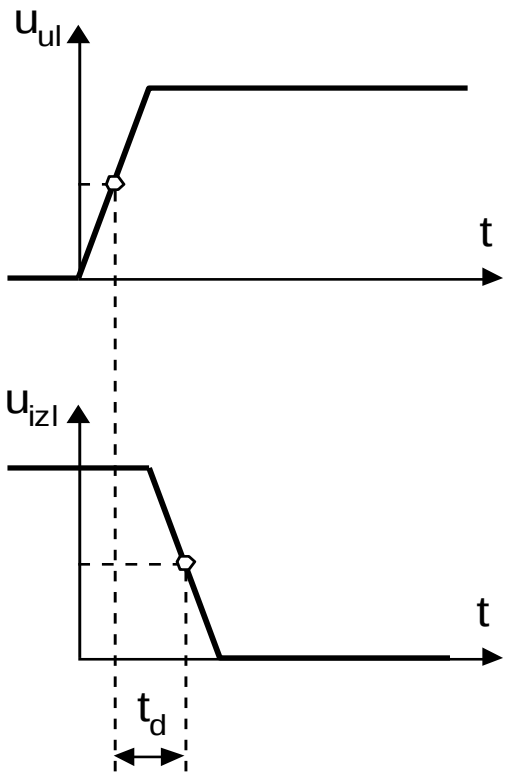
(b) Function table

Vremenski odziv NI sklopa

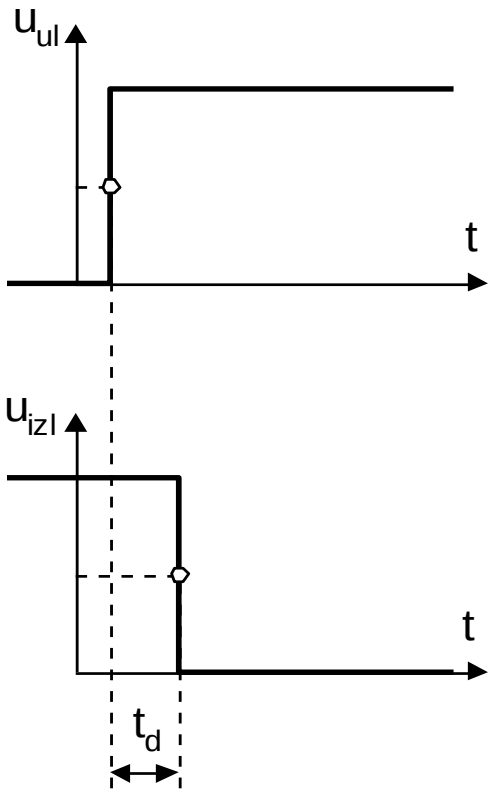


U_u = ulazni napon
U_{izl} = izlazni napon
t_d = vrijeme kašnjenja (time of delay)

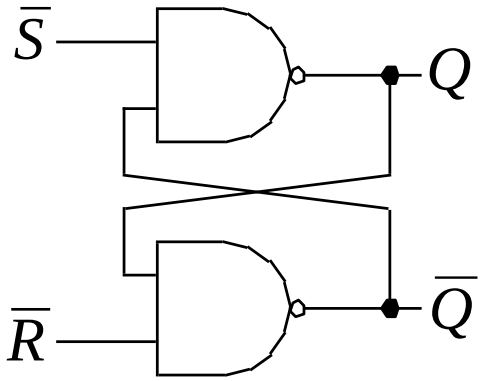
a) Linearna promjena



b) Idealizirana promjena

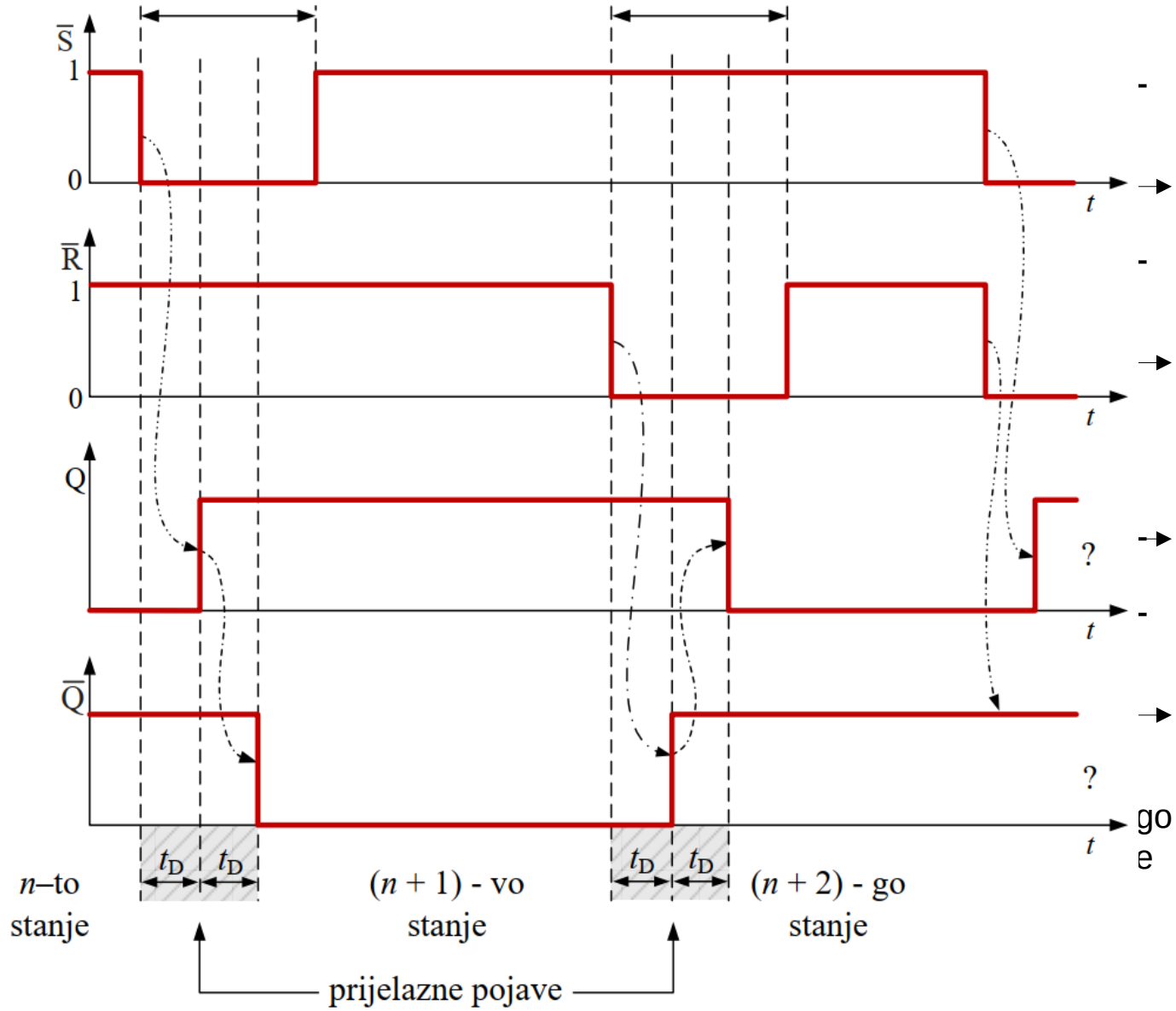


Vremenski odziv bistabila



Sklop je osjetljiv na trajanje pobude (okidnog impulsa):
$t > 2t_D$

Moguć HAZARD!

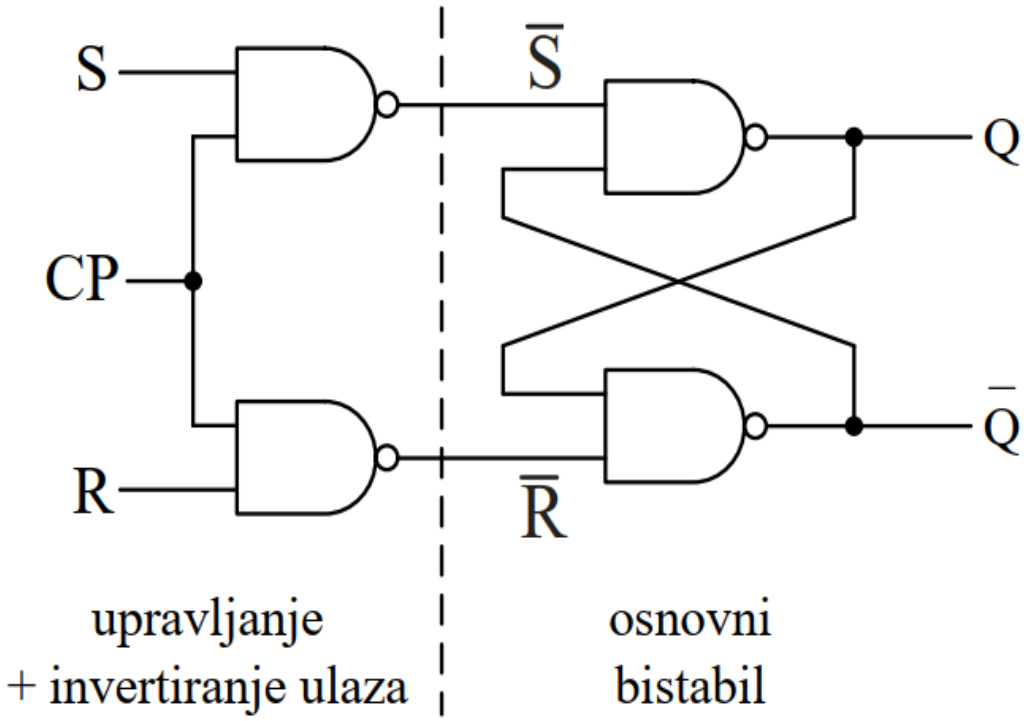


Sekvencijski sklopovi

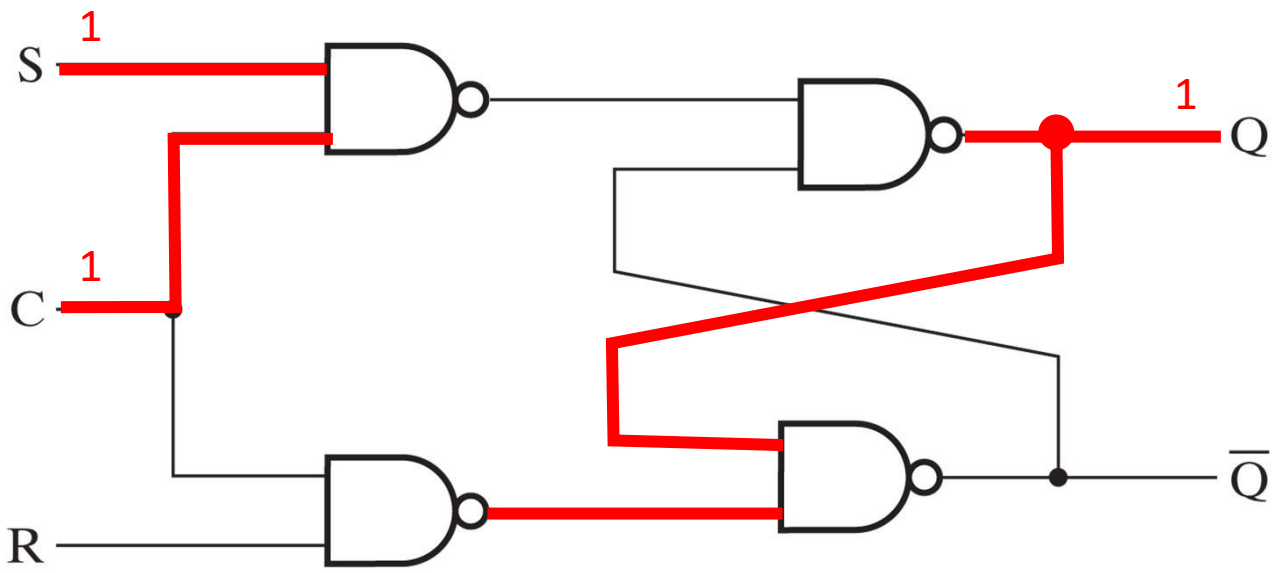
- Mijenjaju stanje pod utjecajem impulsa takta
- Stanje sklopa se može promijeniti samo u određenim trenutcima, čime se izbjegavaju negativni učinci prijelaznih pojava
- Pohranjena binarna informacija definira stanje sekvencijskog sklopa u promatranom trenutku.
- Sekvencijski sklop prima binarne informacije iz svog okruženja putem ulaza
  - Binarna vrijednost izlaza određena je stanjem ulaznih varijabli i pohranjenim stanjem

Sinkroni bistabil

- Na poseban ulaz sinkronog bistabila se dovode sinkronizacijski impulsi **CP** (engl. Clock Pulses)
- Promjena stanja bistabila je moguća samo kad je CP=1
- Ulazi su invertirani, odnosno $\overline{S}\,\overline{R} \rightarrow S\ R$



Sinkroni bistabil

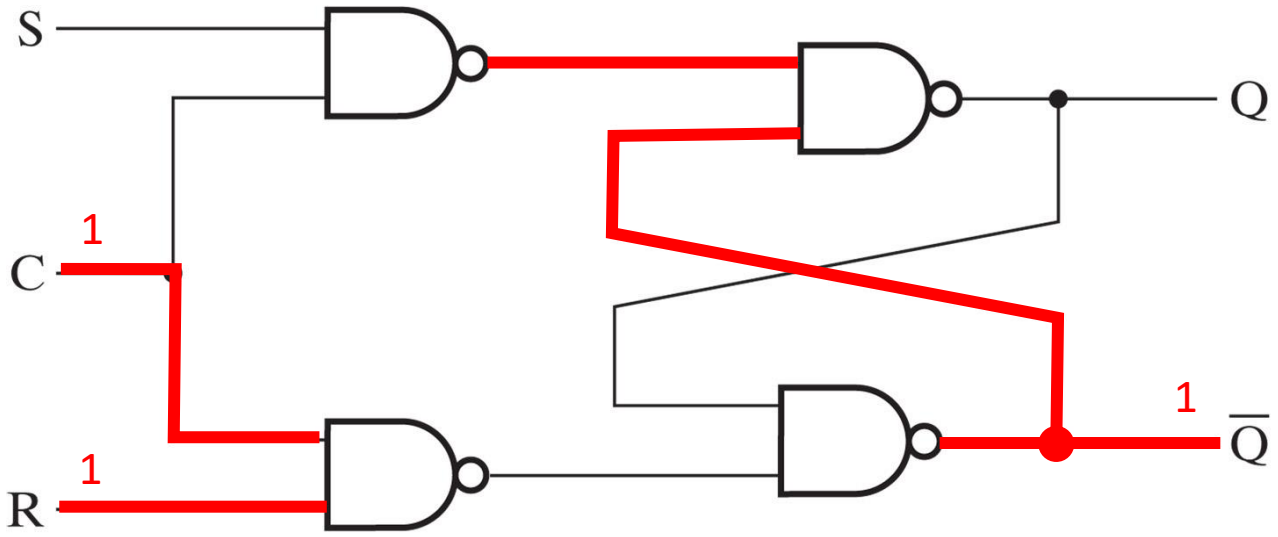


(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

(b) Function table

Sinkroni bistabil



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

(b) Function table

Sinkronizacija okidanja bistabila

Asinkroni bistabil

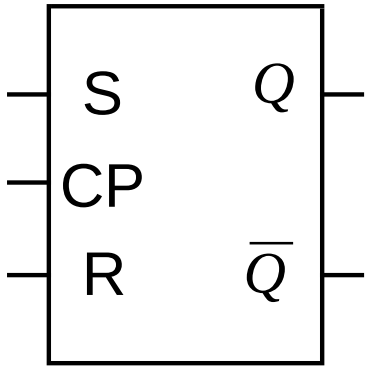
- reagira na promjenu impulsa čim se impuls pojavi na ulazu u sklop, što daje pogrešan rezultat ako se ulazni impulsi ne dovode istovremeno na ulaz

Sinkroni bistabil

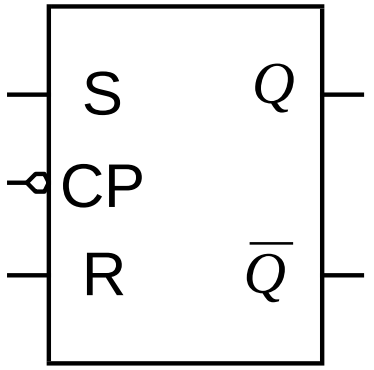
- verzija asinkronog bistabila s dodatnim ulazom CP
- Na ulaz CP (eng. *Clock Pulse*) se dovode sinkronizacijski impulsi konstantne frekvencije
- CP sinkronizira promjene stanja na ulazima bistabila

Sinkronizacija okidanja bistabila

- konceptualno: *diskretizacija* vremena
- značajno olakšava razmatranje sekvencijskih sklopova
  - sekvencijski se problem svodi na kombinacijski
- obično se razmatra prijelaz iz stanja (n) u stanje (n+1)
  - prije (n), odnosno poslije nailaska CP impulsa (n+1)
- aktivna razina okidanja bistabila može biti 0 ili 1
  - aktivna razina 0 se označava kružićem na CP ulazu



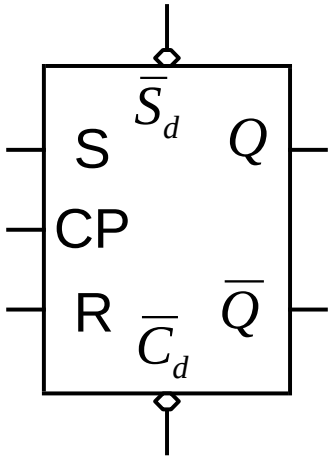
aktivna 1

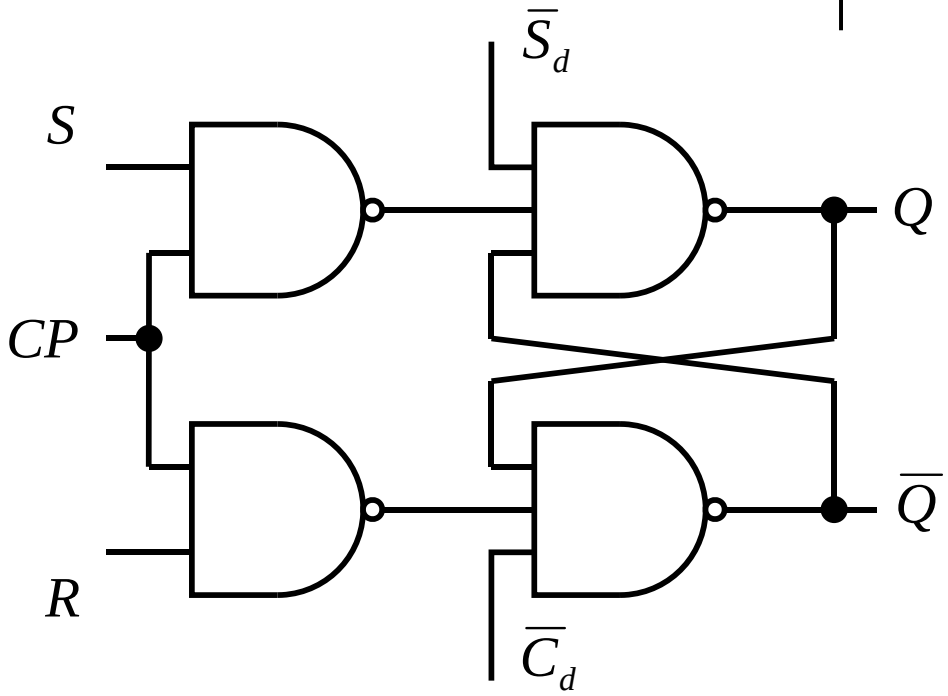


aktivna 0

Dodatni asinkroni ulazi

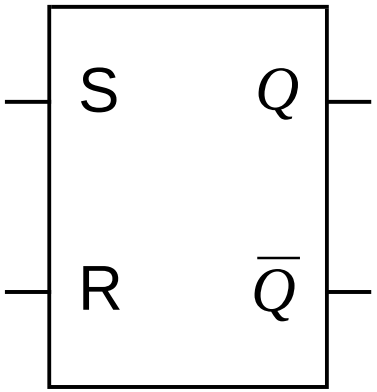
- Omogućuju zaobilaženje sinkronizacijskih impulsa
  - direktni ulazi ($\overline{S_d}$, $\overline{C_d}$)
  - Aktivna razina je 0
  - dominiraju nad sinkronim ulazima S i R
- Potencijalni problem:
  - za vrijeme CP aktivna pobuda putem sinkronih i asinkronih ulaza može izazvati hazard

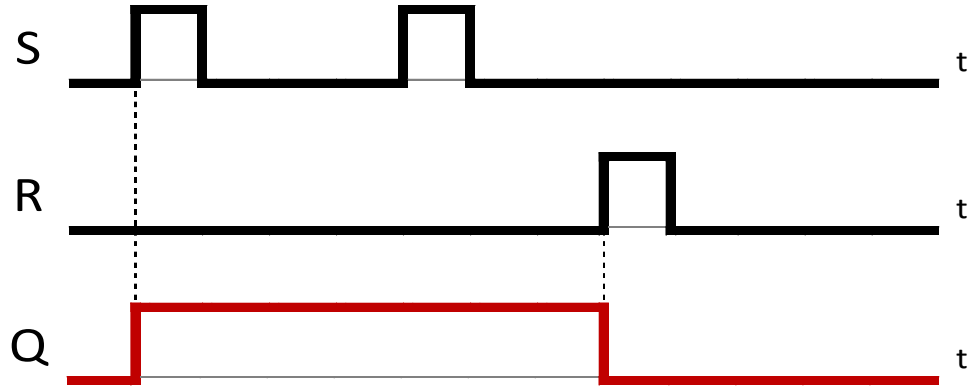




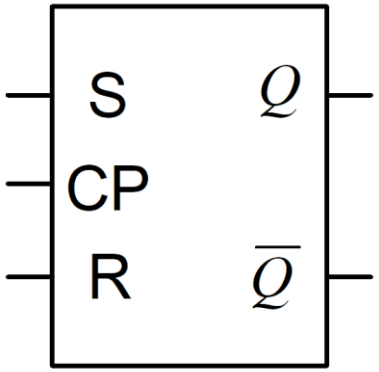
Djelovanje impulsa na SR bistabil

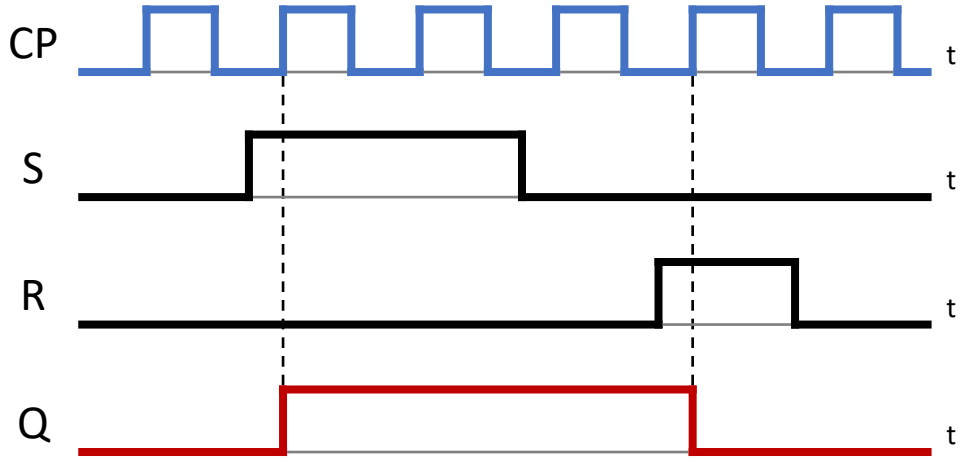
Jednostavni
SR bistabil





Upravljani
SR bistabil





Tipovi bistabila

- **SR** bistabil [set] [reset]
  - osnovna funkcionalnost
- **JK** bistabil*
  - proširena funkcionalnost: "univerzalni" bistabil
- **T** bistabil [toggle]
  - (samo) promjena stanja
- **D** bistabil [delay]
  - (samo) pamćenje 1 bita informacije

* JK bistabil je dobio ime po Texas Instrumentsovom inženjeru Jacku Kilbyju koji ga je osmislio 1958. godine

SR bistabil

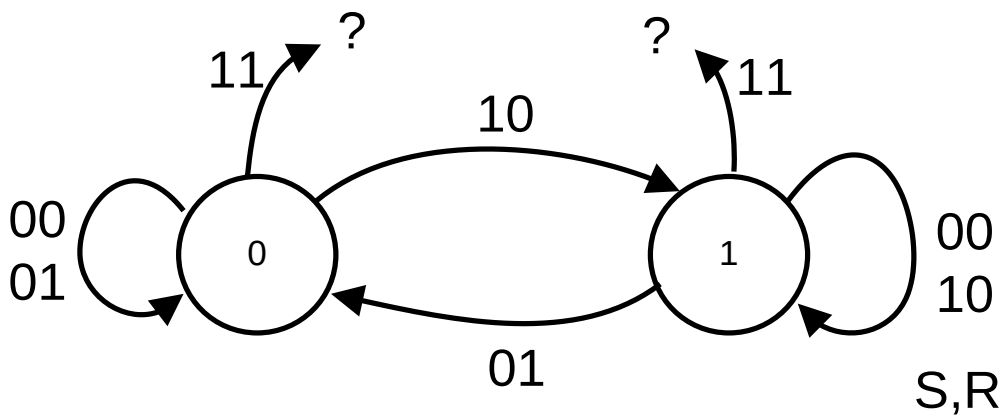
Tablica stanja

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	?, X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	?, X

Sažeta tablica stanja

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

Dijagram stanja

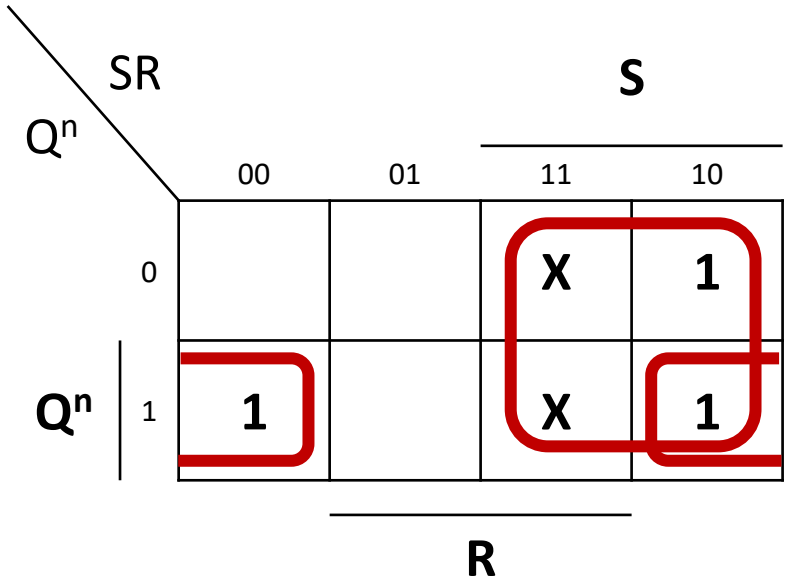


SR bistabil

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	?, X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	?, X

Tablica uzbude predstavlja kombinaciju koja je potrebna da sklop prijeđe iz stanja Q_n u stanje Q_{n+1}

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0



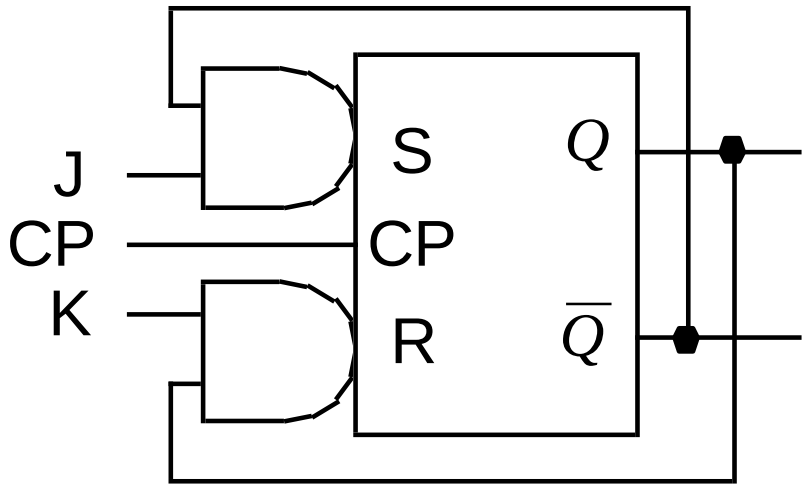
Uvjet $S \cdot R = 0$ omogućuje korištenje **X** u K-tablici

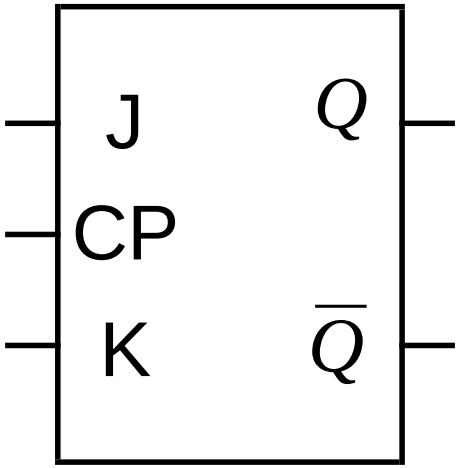
Jednadžba stanja: $Q_{n+1} = S + \bar{R} \cdot Q_n$

JK Bistabil („univerzalni” bistabil)

Rješava problem zabranjenih kombinacija na R i S ulazima

- za JK = 11 bistabil mijenja stanje (engl. *toggle*)
- Izlazi se koriste za upravljanje vlastitim ulazima



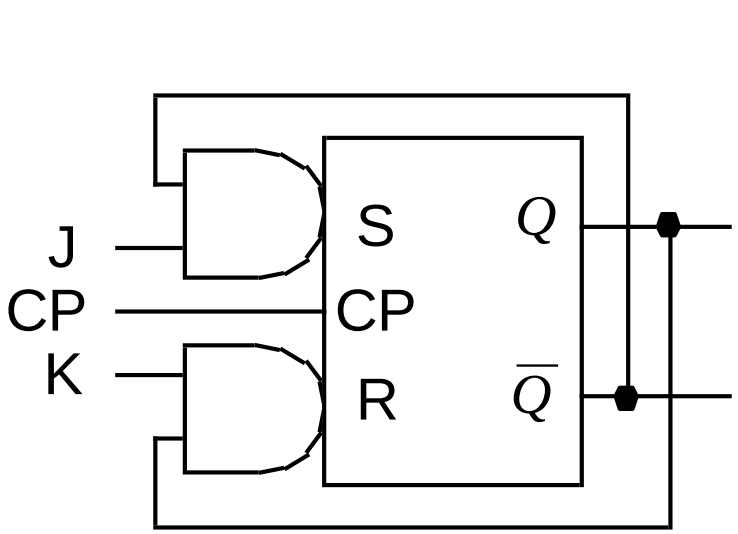


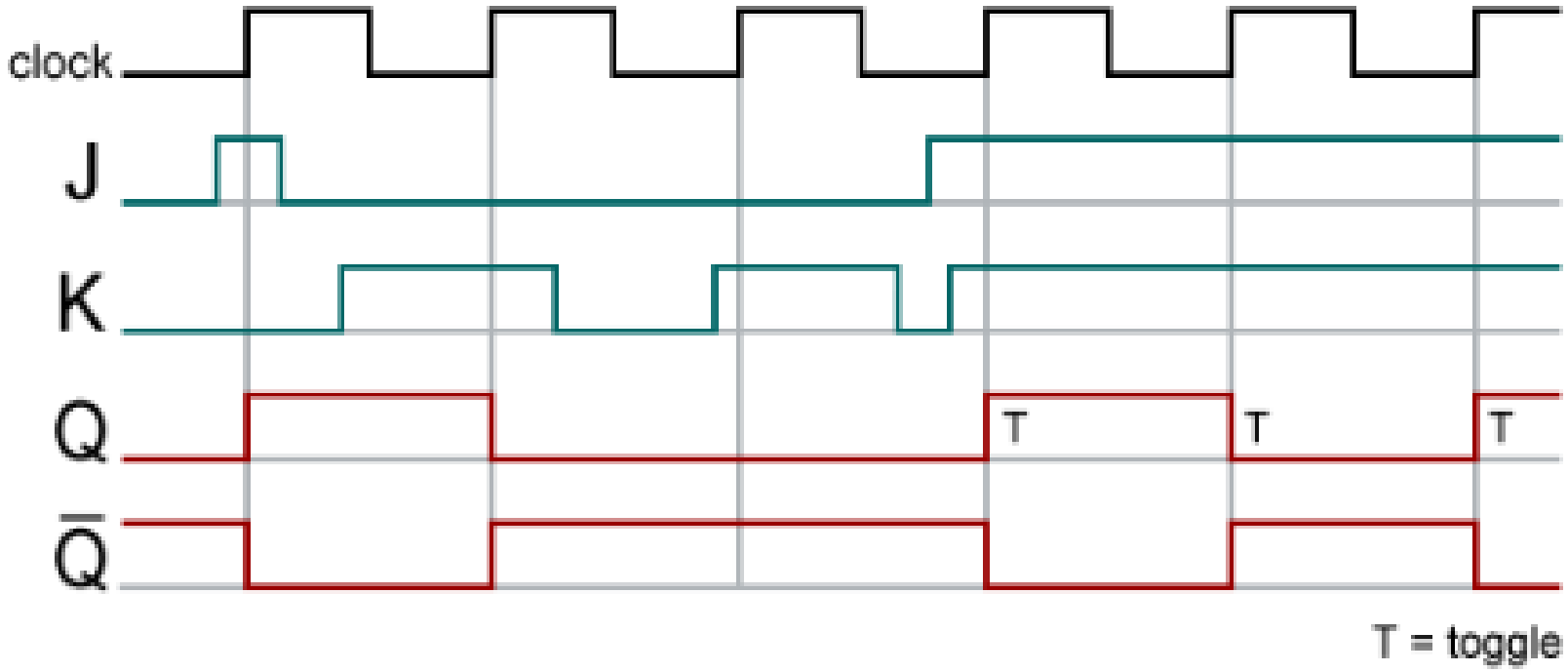
Sažeta tablica:

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

JK bistabil

Primjer vremenskog dijagrama





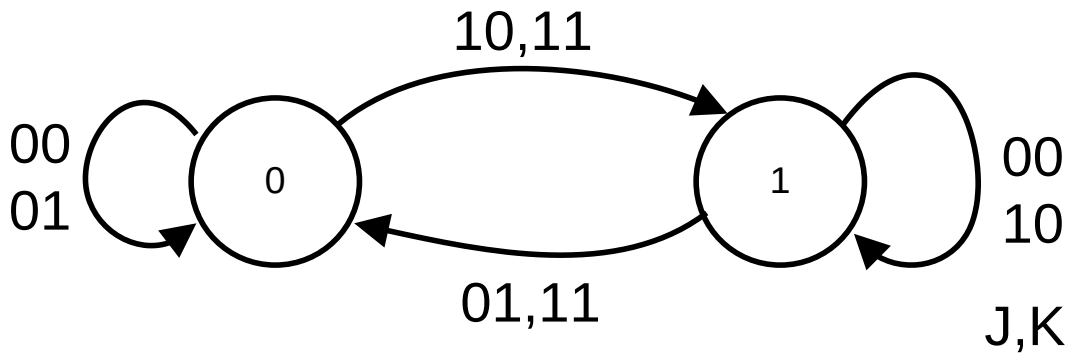
JK bistabil

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Tablica uzbude

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Dijagram stanja

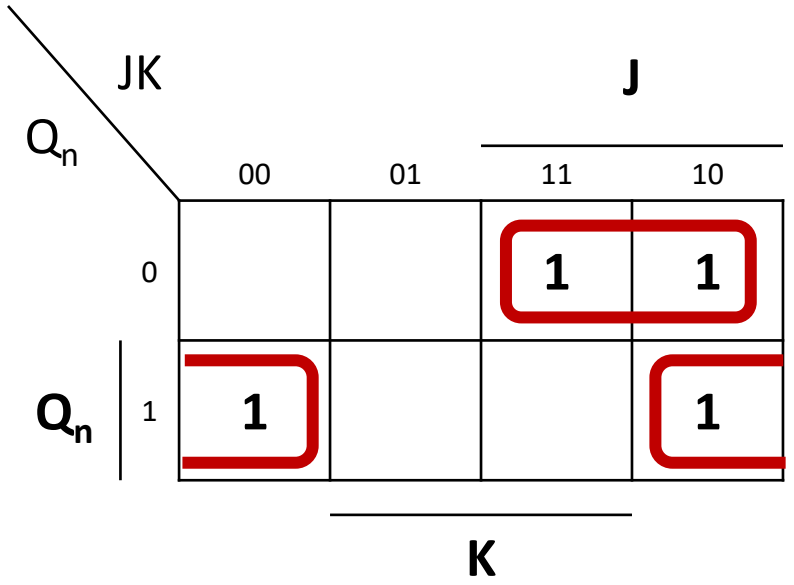


JK bistabil

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Tablica uzbude

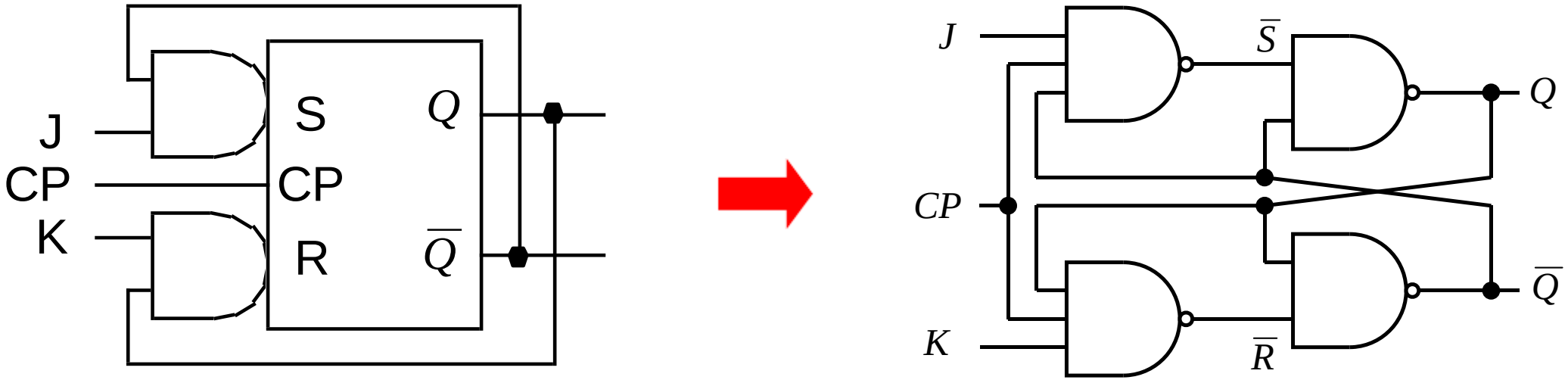
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



Jednadžba stanja:

$$Q_{n+1} = J \cdot \bar{Q}_n + \bar{K} \cdot Q_n$$

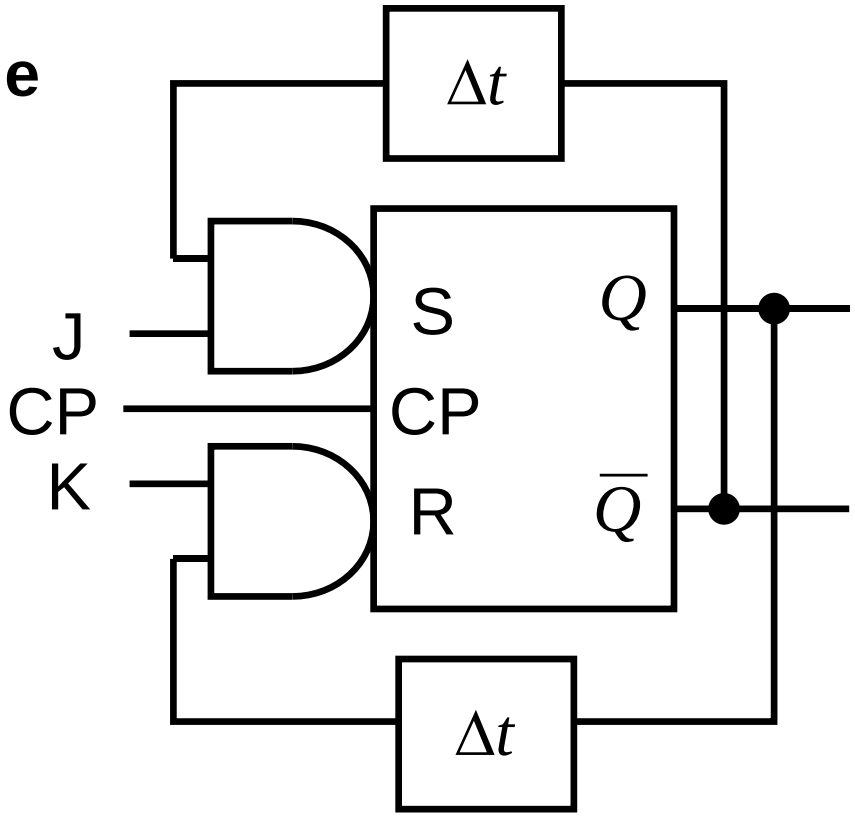
JK bistabil izveden pomoću NI sklopova



CP = 1 ne smije trajati predugo radi opasnosti od osciliranja (neprekidne promjene stanja)

Suprotstavljeni zahtjevi za trajanje CP

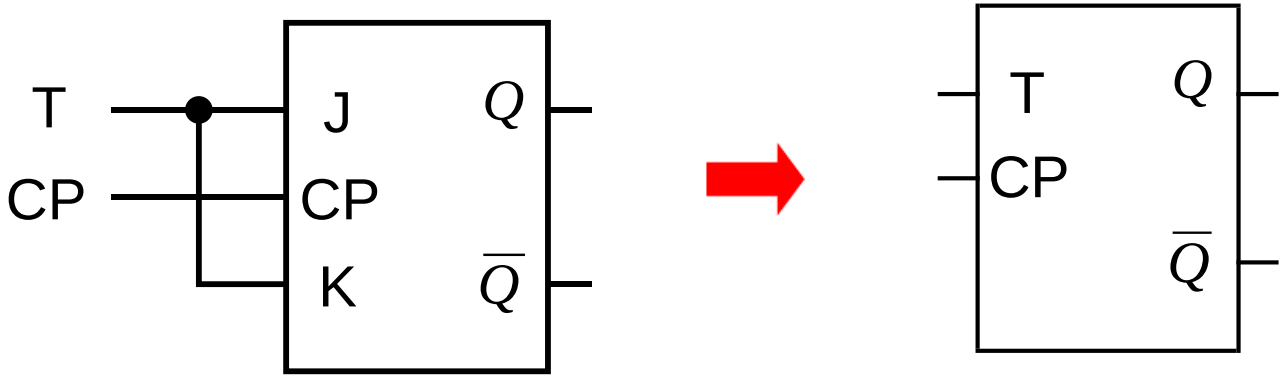
- Dužina CP impulsa mora biti:
  - dovoljno **duga** da bistabil **promijeni stanje**
  - dovoljno **kratka** da bistabil **ne zaoscilira**
- Moguća rješenja:
  - odgovarajuća kašnjenja u petlji povratne veze
  - poboljšano upravljanje djelovanjem na CP



T bistabil (od engl. *Toggle*)

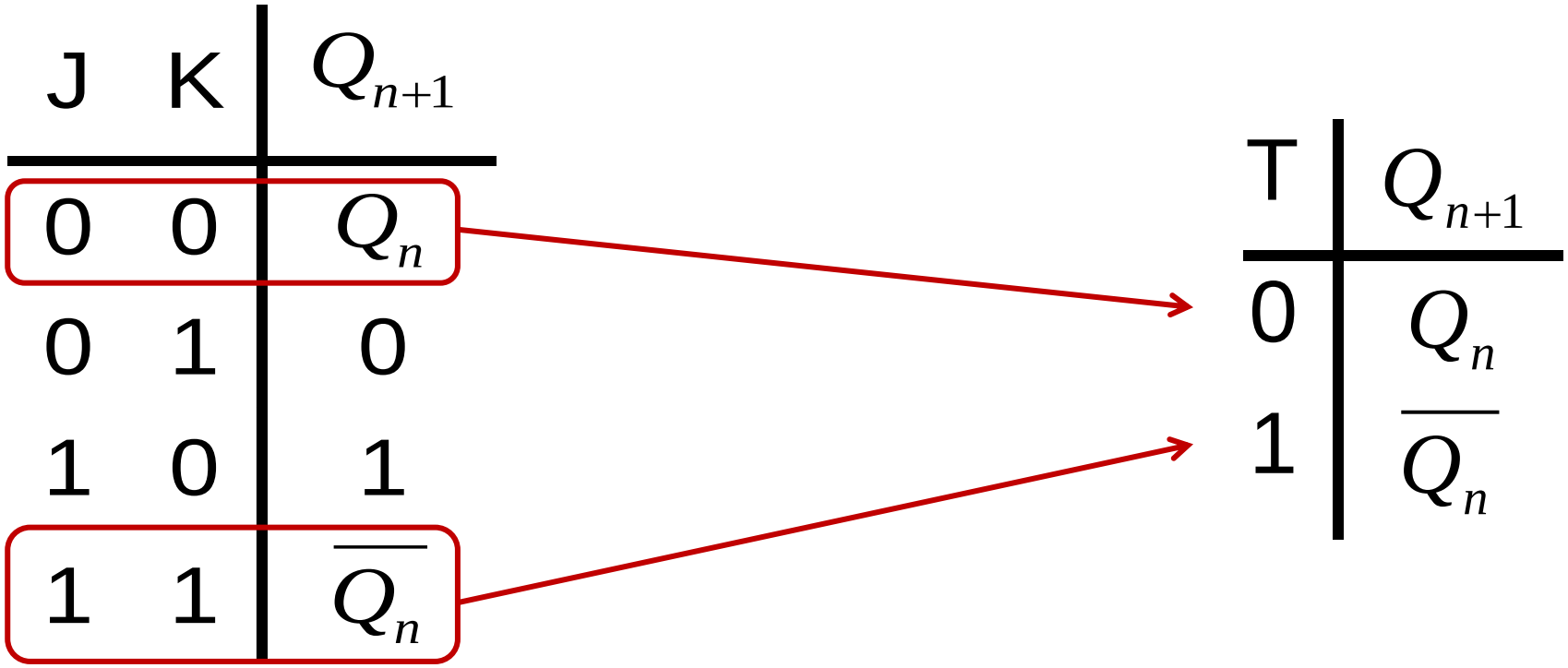
Međusobnim spajanjem J i K ulaza dobivamo **T bistabil**

- Uz T = 0, bistabil mijenja stanje sa svakim CP impulsom
- Tipično se primjenjuje za brojanje impulsa (u sklopovima brojila)



Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

T bistabil



T bistabil

Tablica stanja

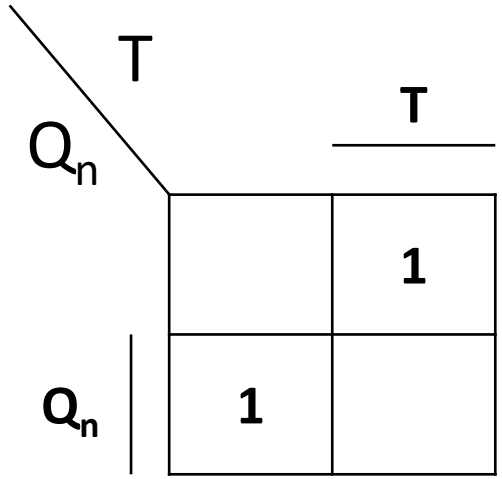
Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

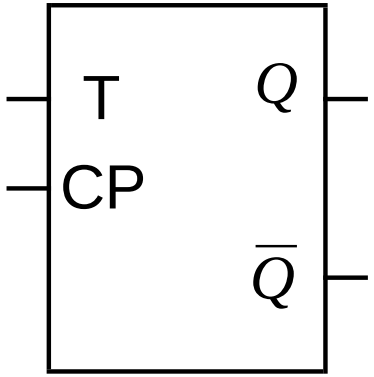
Tablica uzbude

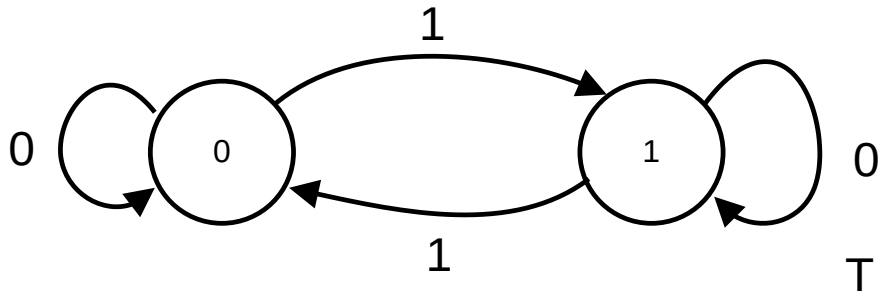
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Sažeta tablica stanja

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$



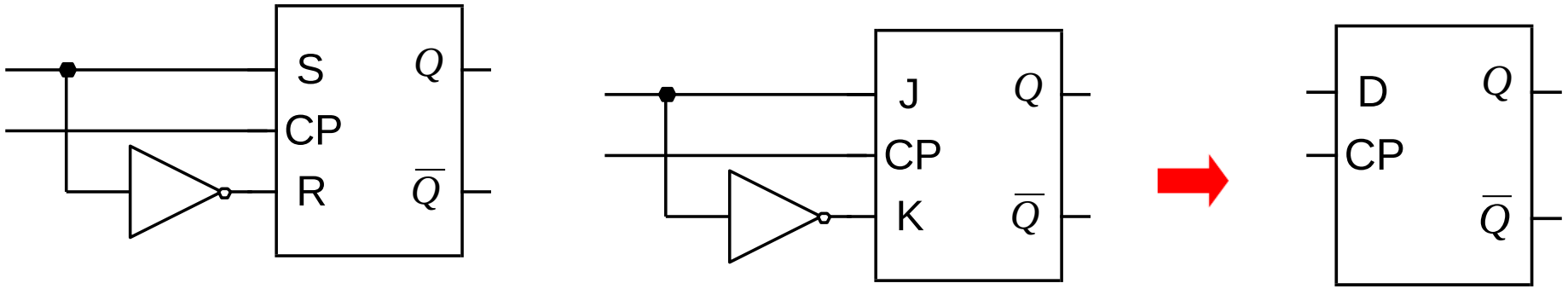




$$Q_{n+1} = T \cdot \overline{Q}_n + \overline{T} \cdot Q_n$$

D bistabil (od engl. *Delay*)

- Međusobnim spajanjem ulaza i invertiranog ulaza na RS ili JK bistabil dobivamo **D bistabil**
- D bistabil pamti (memorira) podatak (jedan ulazni bit)
- Primjenjuje se za:
  - pohranu podataka (registar)
  - kašnjenje (engl. *delay*) za 1 x CP



D bistabil

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

D	Q^{n+1}
0	0
1	1

D bistabil

Tablica stanja

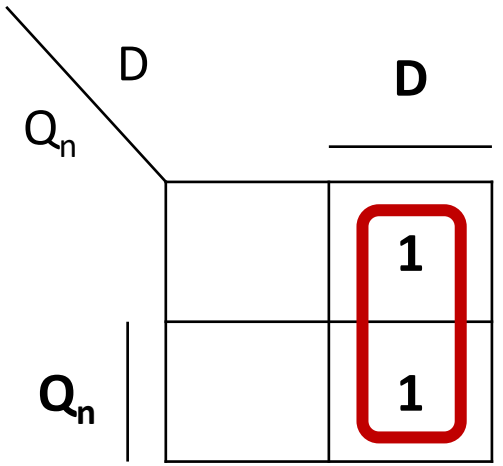
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

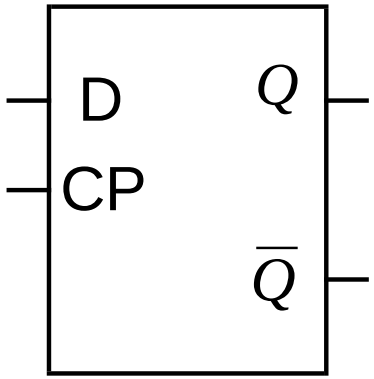
Tablica uzbude

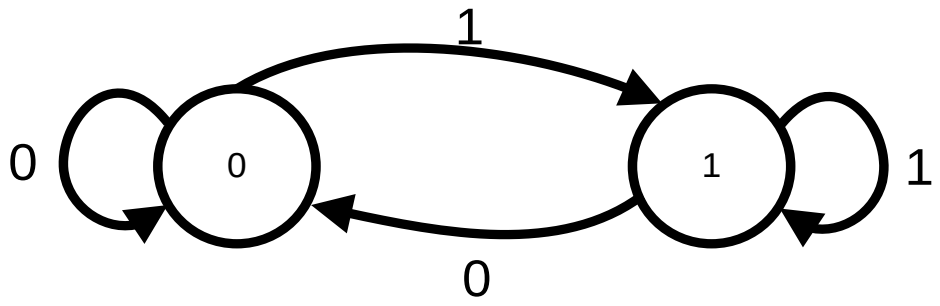
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Sažeta tablica stanja

D	Q^{n+1}
0	0
1	1







$$Q_{n+1} = D_n$$

Prevencija osciliranja JK bistabila

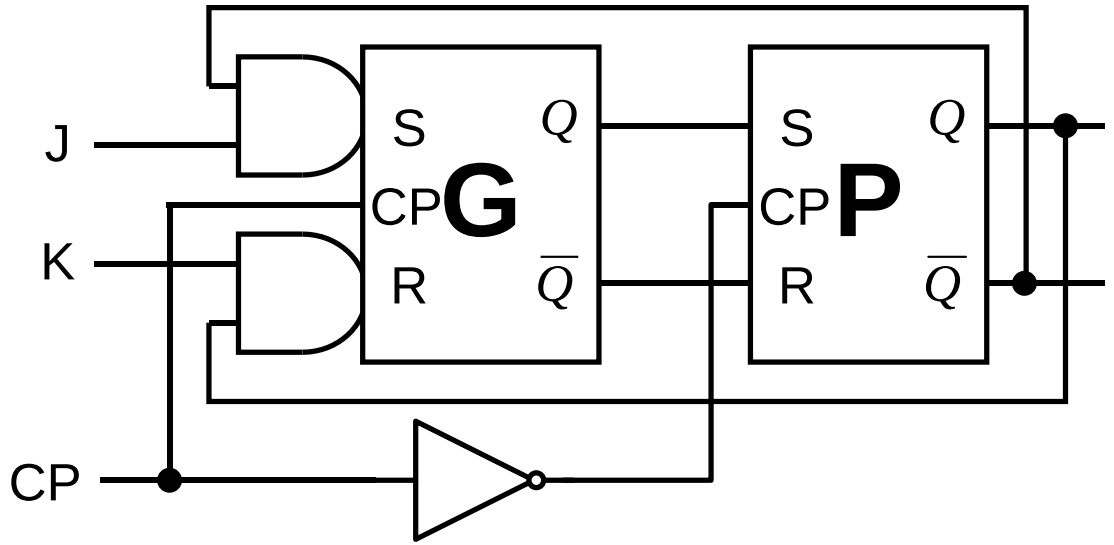
Moguća rješenja za poboljšanje upravljanja putem CP:

- **Razinom okidani bistabil** (engl. *latch*) - daje odziv na svojim izlazima kod **promjene ulazne razine**
- **Bridom okidani bistabil** (engl. *flip-flop*) daje odziv na ulazne promjene samo u vremenskim trenucima **promjene signala takta**
  - Uzima uzorke signala s ulaza samo na bridovima signala takta
  - Stanja izlaza se mijenjaju isključivo kao rezultat pojave brida signala takta

Dvostruki bistabil *(master-slave flip-flop)*

Upravljanje **razinom** CP:

1. CP = 0
   - glavni (G) i pomoćni (P) bistabil su povezani (CP=1)
2. CP = 1
   - u glavni bistabil se upisuje novi sadržaj
3. CP = 0
   - sadržaj glavnog bistabila se prenosi u pomoćni bistabil

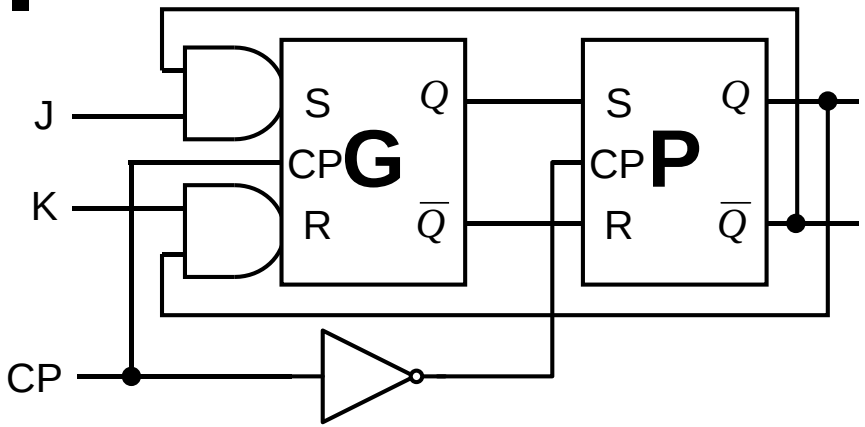


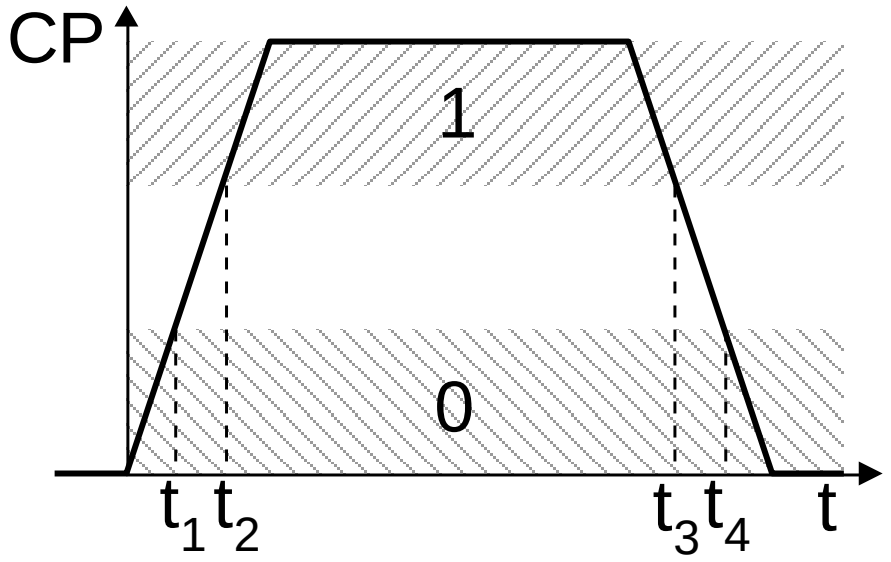
Razinom okidani bistabil

Princip rada:

- t_1: CP izlazi iz područja **0**:
  prekid veze G i P
- t_2: CP ulazi u područje **1**:
  uspostavljanje veze ulaza i G,
  upis podataka u G
- t_3: CP izlazi iz područja **1**:
  prekid veze ulaza i G
- t_4: CP ulazi u područje **0**:
  uspostavljanje veze G i P,
  upis podataka iz G u P

Osciliranje je onemogućeno





Bridom okidani bistabil *(edge-triggered flip-flop)*

Upravljanje **bridom** CP:

- Bistabil ignorira postojano stanje CP-a - okida samo tijekom tranzicije stanja 1→0 ili 0→1, ovisno o izvedbi

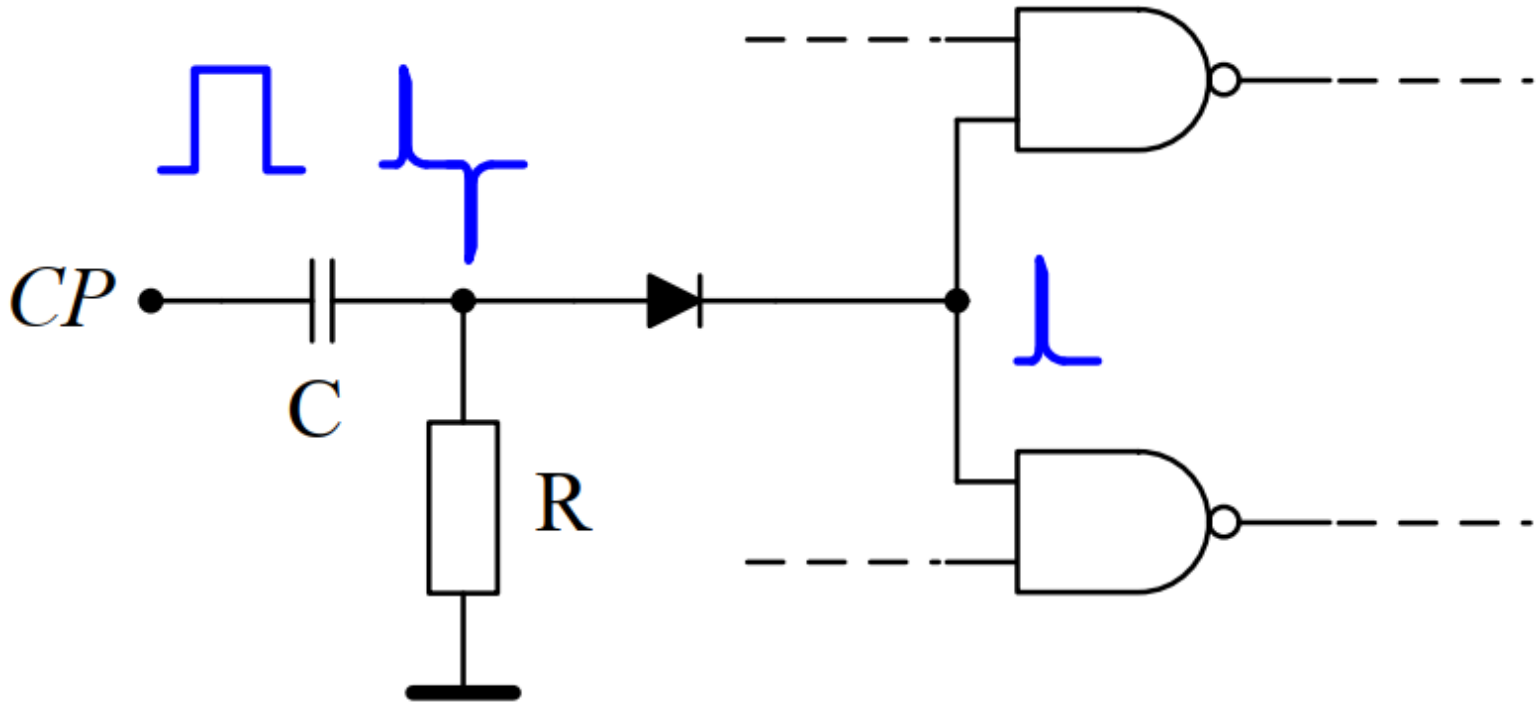
Osnovna ideja:

- na jedan od bridova impulsa CP generirati **kratki impuls** koji će propustiti ulaze
- više mogućih izvedbi
  - korištenje **CR mreže**
  - korištenje **kašnjenja u logičkim sklopovima**
  - kombiniranje **većeg broja osnovnih bistabila**

Kreiranje impulsa CR mrežom

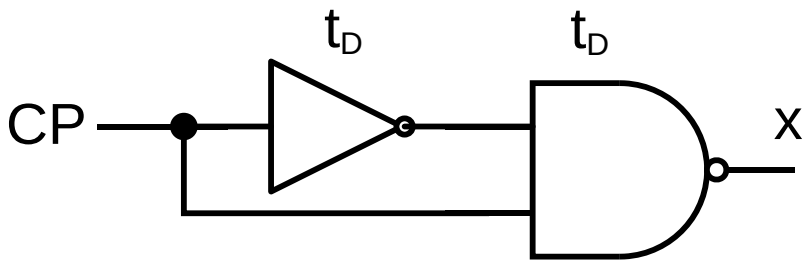
MrežaCR - deriviranje impulsa CP

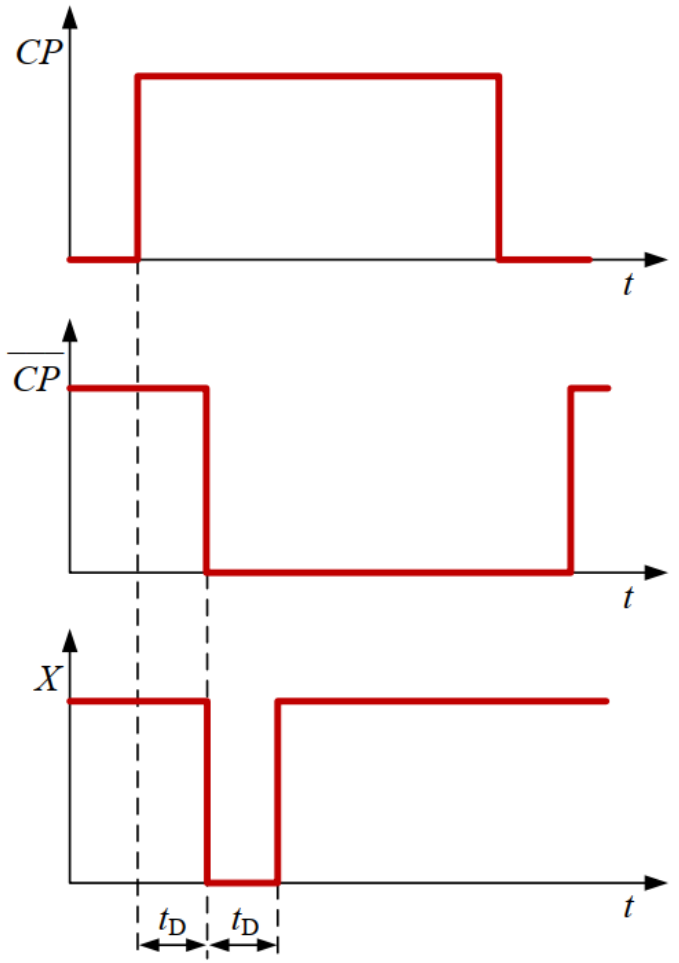
- nije prikladno za integriranu izvedbu



Kreiranje impulsa kašnjenjem

Korištenje kašnjenja u logičkim sklopovima

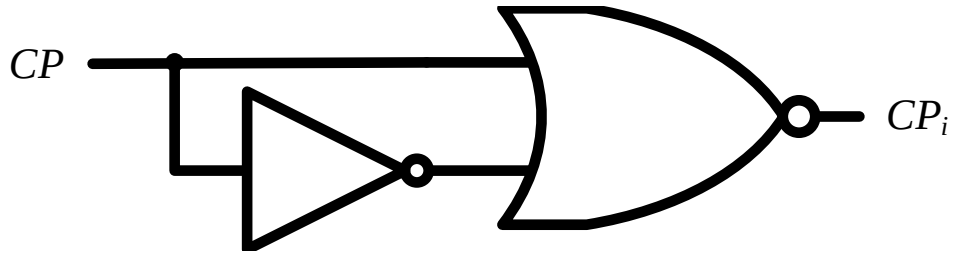


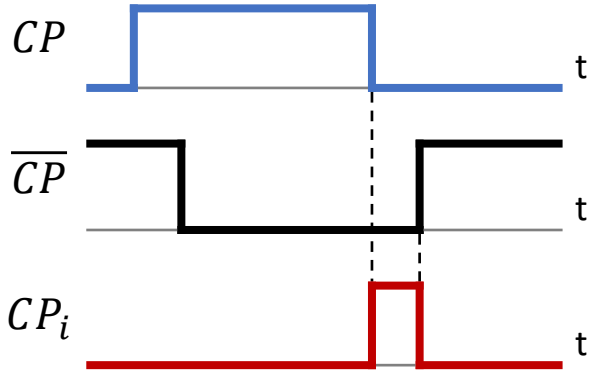


Na rastući brid impulsa CP generira se impuls trajanja t_d

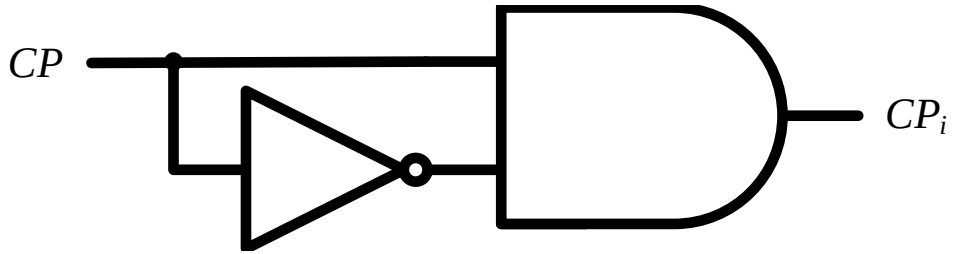
Sklopovi za detekciju brida

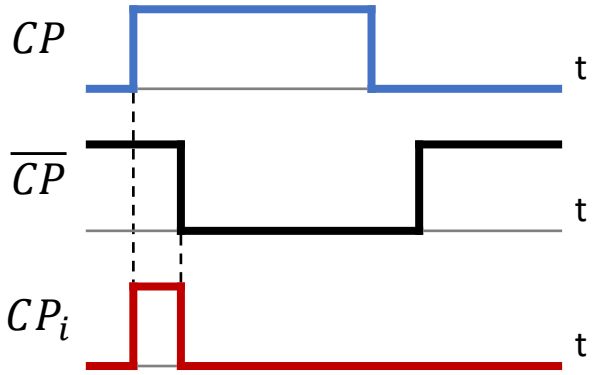
- Sklop za detekciju padajućeg brida



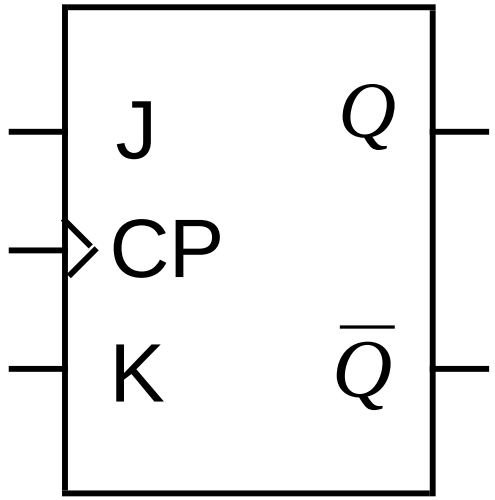


- Sklop za detekciju rastućeg brida

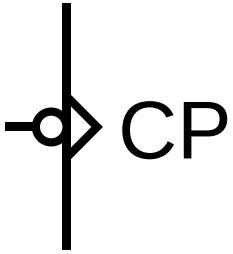




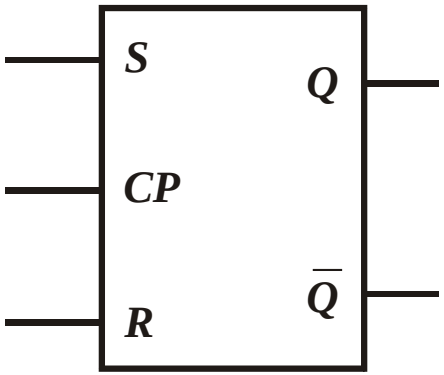
Bridom okidani JK bistabil

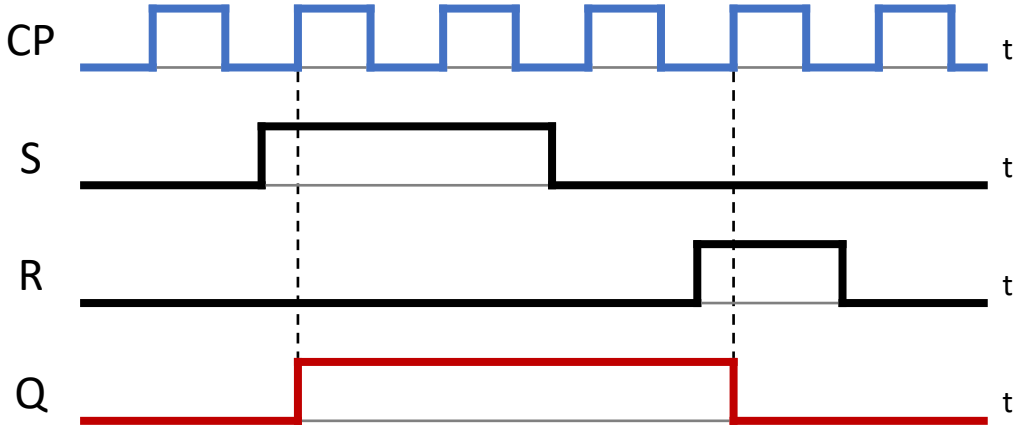


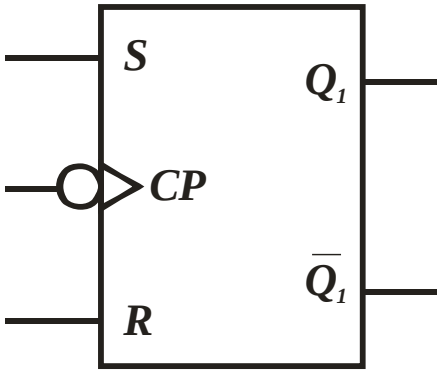
Simbolički prikaz okidanja negativnim bridom:

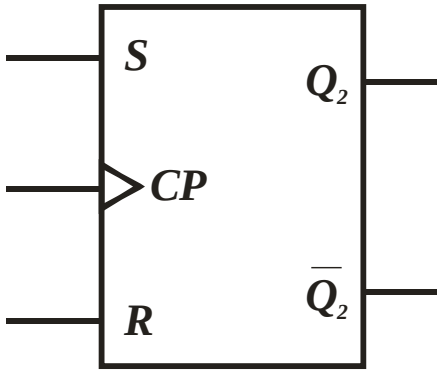


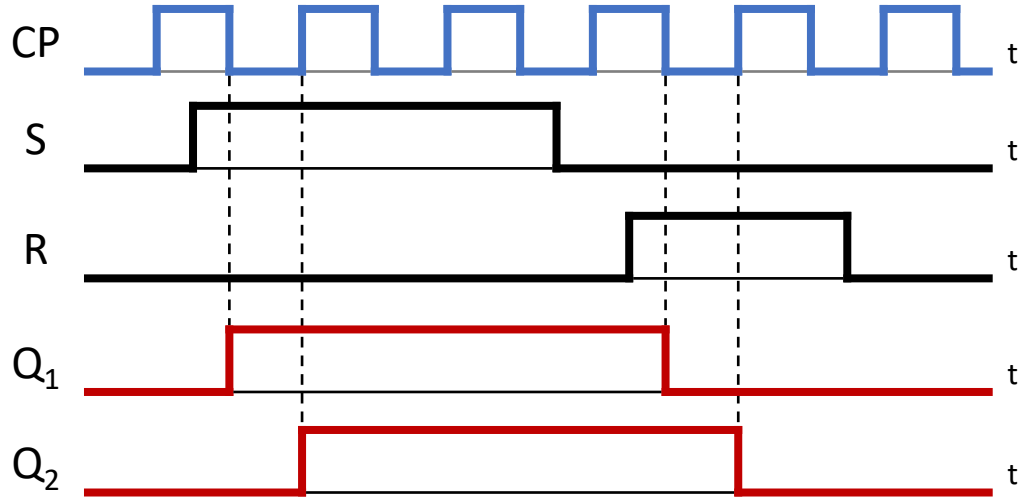
Usporedba upravljanja razinom i bridom



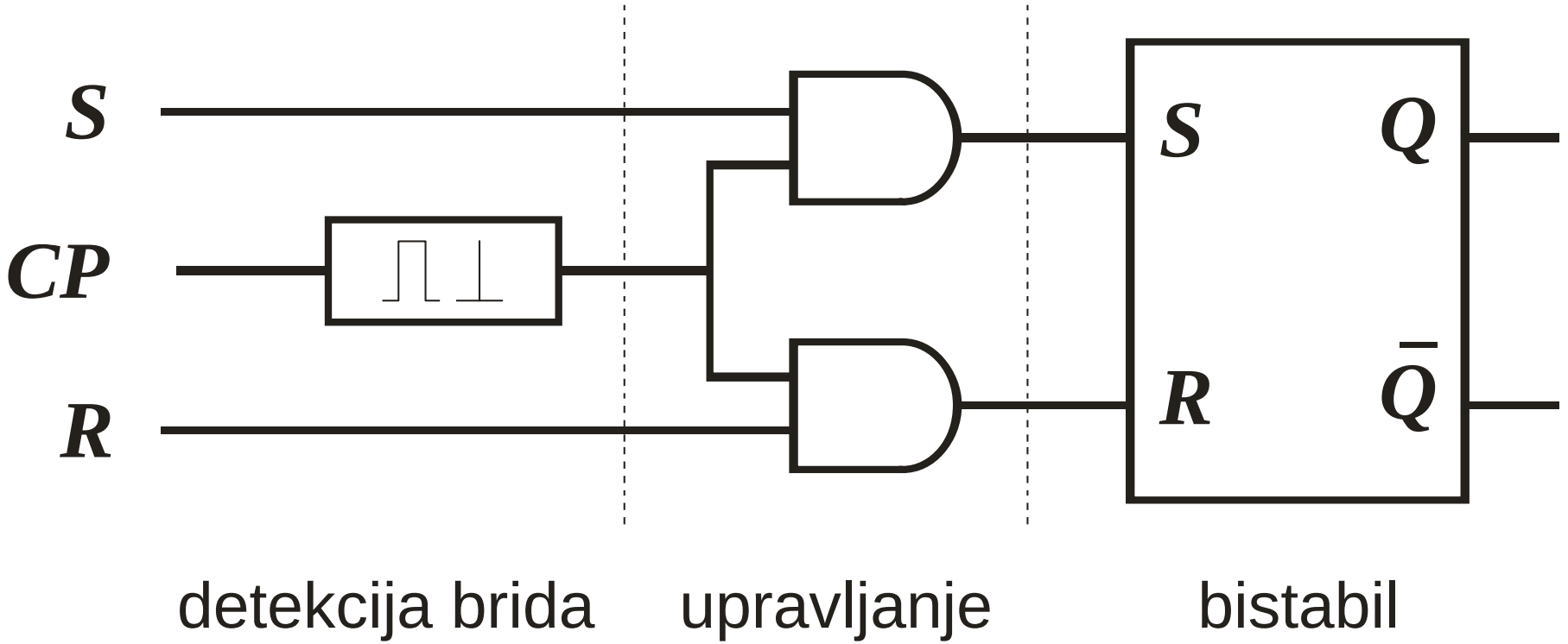




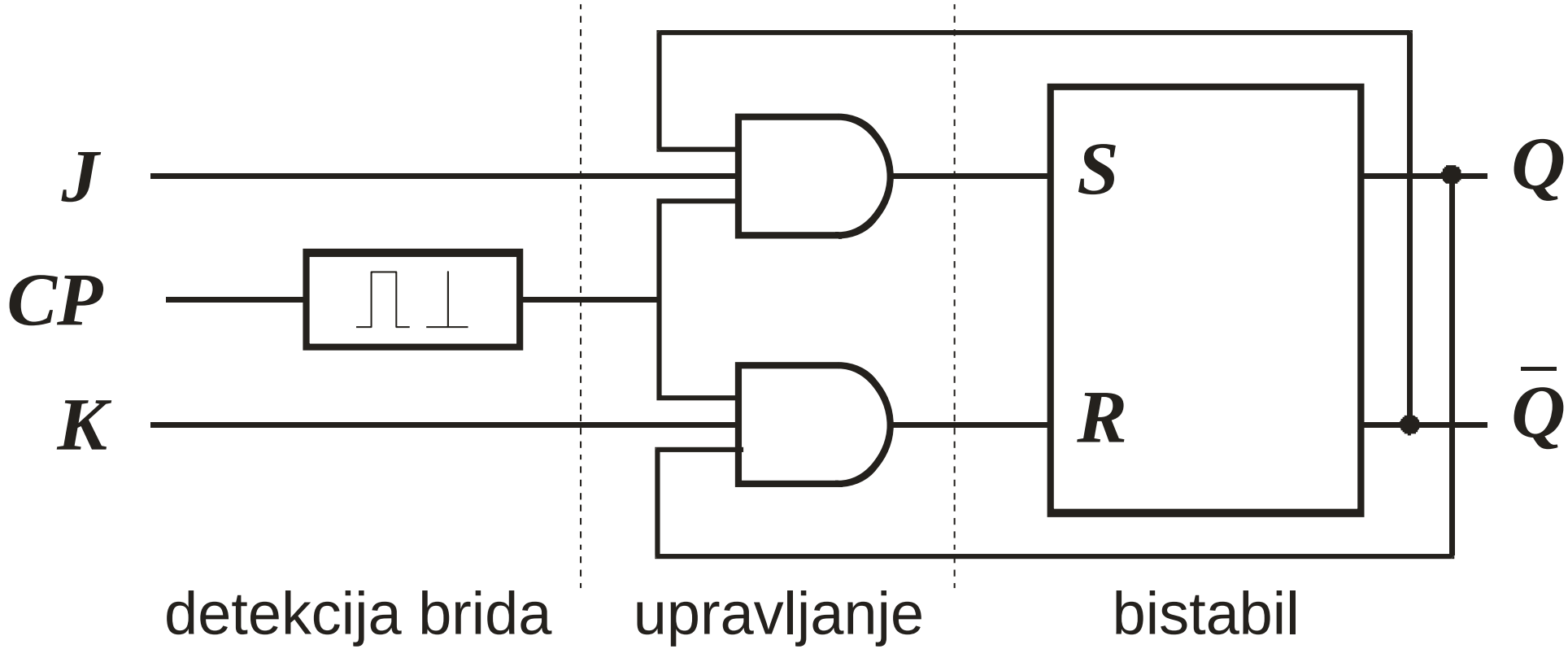




Logička shema bridom upravljanog SR-bistabila



Logička shema bridom upravljanog JK-bistabila

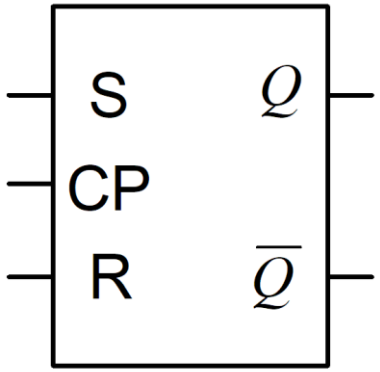


Bistabili

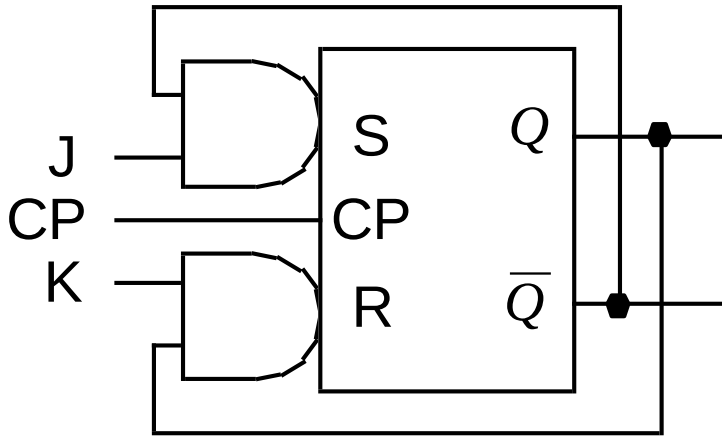
LITERATURA:

- Uroš Peruško: Digitalni sustavi
  - Str. 165 - 198

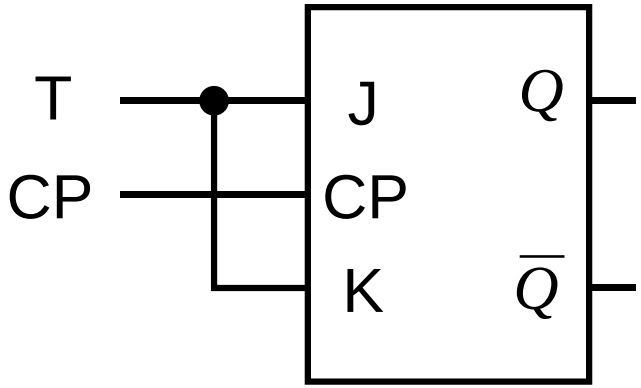
SR


S
CP
R
Q
$\overline{Q}$

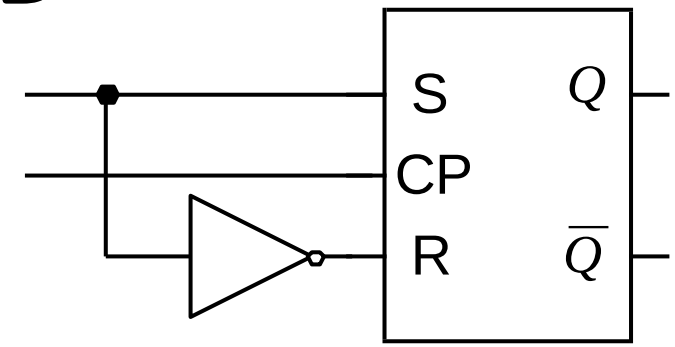
JK


J
CP
K
S
CP
R
Q
$\overline{Q}$

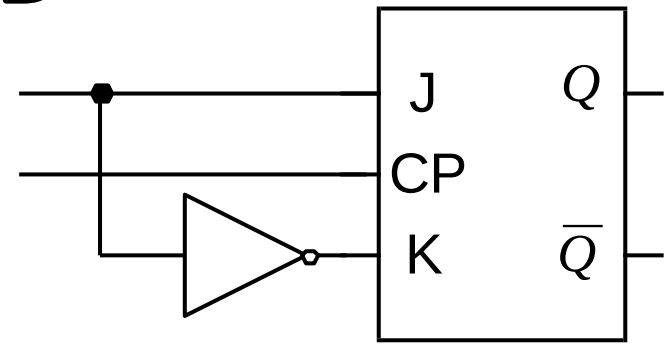
T


T
CP
J
CP
K
Q
$\overline{Q}$

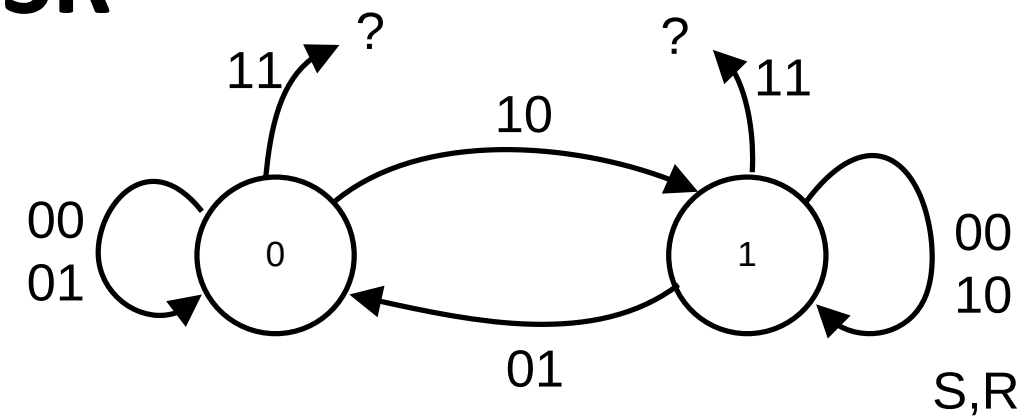
D


S
CP
R
Q
$\overline{Q}$

D


J
CP
K
Q
$\overline{Q}$

SR


11
?
10
?
11
00
01
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1
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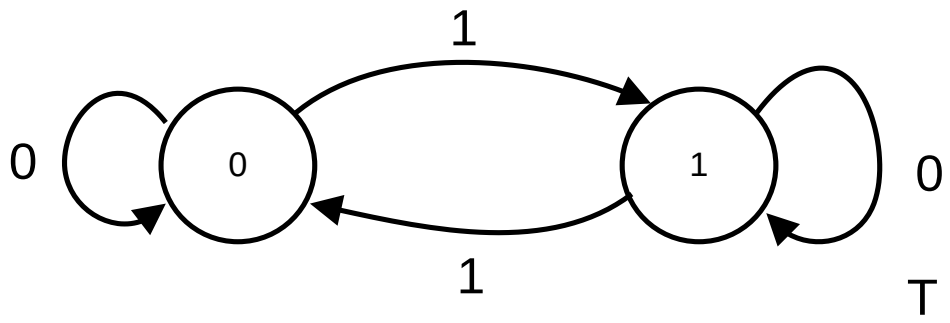
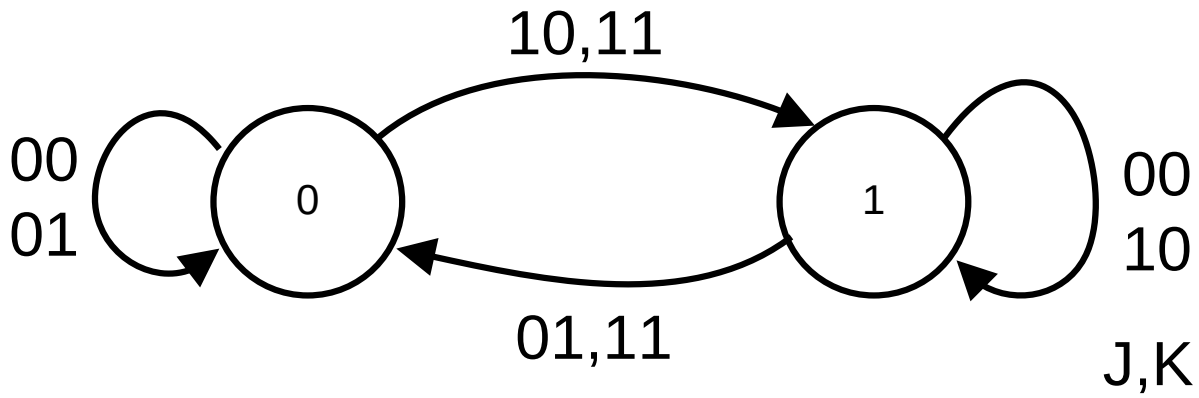
01
S,R

T


1
0
0
1
0
1
T

JK


10,11
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01
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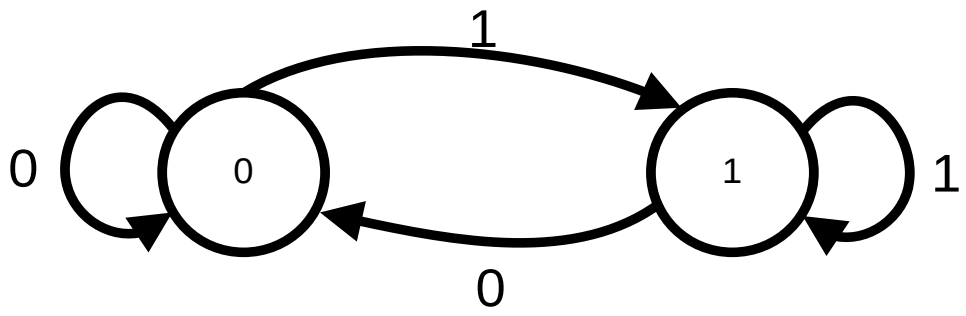
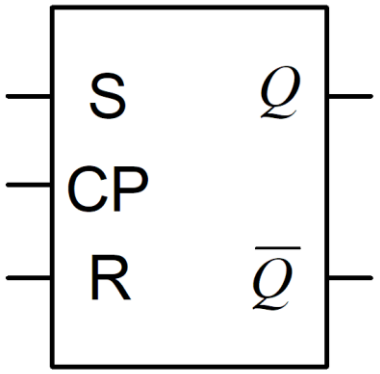
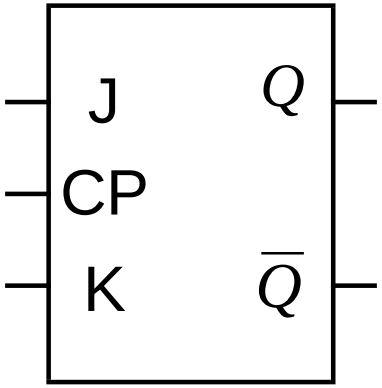
1
00
10
01,11
J,K

D

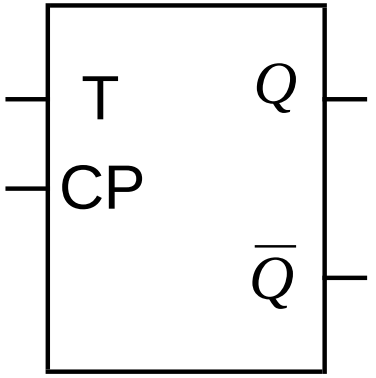

1
0
0
1
1
0
D



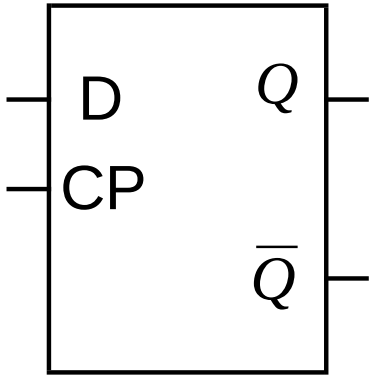
Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X



J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$



T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$



D	Q^{n+1}
0	0
1	1